The University of Alberta

Sub-1V Supply Voltage References for CMOS Technology Based on Threshold-Voltage-Difference Architecture

by

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Abstract

This thesis discusses one class of the nonbandgap voltage references based on threshold-voltage-difference architecture.

The considered voltage references exploit weak temperature dependence of the difference of MOS transistor threshold voltages. This difference is nearly constant across a wide range of temperatures -20 to 120°C. This fact is used to design voltage references with a low power supply voltage (below 0.8 V) in modern 0.18-micron CMOS technology. The theoretical investigation and simulations show that their temperature operation range is very wide (-25 to 125°C), and the power supply voltage may change simultaneously from 1.8 V down to 0.6 V. The variation of the output voltage in this temperature range and power supply range is as low as 0.7%. The references have a simple schematic and may be easily designed.

The practical realization of these references was, in out case, limited by the availability of devices realizable as a CMC multi-project university chip. In these chips only n- and p- channel regular and n-channel native (or so-called "natural") transistors are available. The thesis outlines the theory of considered voltage references, and gives the results of simulation of two representative examples of these references. At the time of writing, two reference circuits have been submitted to CMC for fabrication, and the chips will arrive in January 2006 for testing and measurements.

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List of Symbols

I_C	The collector current
I_S	The saturation current
V_{BE}	The base-emitter voltage
V_T	The thermal voltage
N_A	Acceptor concentration
W	Width of a MOS transistor gate
V_{g0}	The bandgap voltage of silicon extrapolated to 0°K
Q_{SS}	The surface-state charge density per unit area
C_{ox}	Gate oxide capacitor per unit area
ϕ_{ms}	Metal-semiconductor work function difference
ϕ_F	Fermi level
N_i	Impurity concentration
N_s	Substrate doping
γ	The body-effect constant
t_{ox}	The gate oxide thickness
V_0	A correction term owing to the threshold shift implant
L	Length of a MOS transistor gate
n_c	Carrier concentration
n_i	Intrinsic carrier concentration
N_D	Donor concentration
T	Absolute temperature
V_{TH}	Threshold voltage
α_{VT}	Temperature coefficient of the threshold voltage
μ	Carrier mobility
μ_n	Mobility of majority carriers (electrons) in n-channel

μ_p	Mobility of majority carriers (holes) in p-channel
T_0	The reference temperature
N_D	Donor concentration
N_A	Acceptor concentration
N_P	Carrier concentration in the poly-silicon gate
I_{DF}	The temperature-independent drain current
V_{GS}	The gate-source voltage
V_{GSF}	The temperature-independent voltage
q	Electron charge ($q = 1.6 \cdot 10^{-19}$ Coulomb)
k	Boltzmann constant ($k = 8.62 \cdot 10^{-5}$ eV/°K)
kT	Thermal energy
I_B	The bias current
I_D	The drain current
J_S	Saturation current density
Q_i	The implanted charge per unit area
V_{DD}	The power supply voltage
$V_{DD\,min}$	Minimum required power supply
V_{SD}	The source-drain voltage
V_{SDsat}	The saturated source-drain voltage
V_{REF}	The reference voltage
V_{SB}	The source-body voltage
V_{THp}	PMOS threshold voltage
V_{THn}	NMOS threshold voltage
α_{R1}	First order temperature coefficient of a resistor
α_{R2}	Second order temperature coefficient of a resistor
μ_e	Electron mobility
μ_h	Hole mobility

Chapter 1 Introduction

1.1 Motivation

Most, if not all, electronic circuits and systems use a reference, be it voltage, current or time. A reference in a circuit establishes a stable point used by other sub-circuits to generate predictable and repeatable results. This reference point should not change significantly under various operating conditions. Temperature is an important parameter that affects the performance of references. Special attention should therefore be paid to the temperature behavior of the reference. The typical metric used for variations of the reference voltage with temperature is the temperature coefficient (TC), which is normally expressed in parts-per-million per degree Celsius (ppm/°C),

$$TC_{ref} = \frac{1}{\text{Reference}}\left(\frac{\partial \text{Reference}}{\partial \text{Temperature}}\right) \tag{1.1}$$

where the "Reference" is either in volts, amperes, or seconds [1].

Current references are used in most of the basic building blocks [2]. Usually, the current in different basic blocks results from mirroring of one or more reference currents. Therefore, it is important that the master current of the system be power-supply independent, and designed with the required accuracy. Current references are also used for the design of voltage references. A current reference typically does not need to be temperature-independent, however, its temperature coefficient should be well characterized and controlled.

Voltage references have been used in various fields of application, for example, in digital-to-analog (D/A) converters, the automotive industry, and in battery-operated DRAMs [3]. In D/A converters, depending on the digital input word, the analog voltage is a fraction of the internal reference voltage. As for many applications, this digital-to-analog conversion should not depend on temperature, so the reference voltage has to be temperature-independent. Nowadays, high-resolution D/A converters are be-

ing used, and, consequently, the reference voltage must be very stable as each variation in the reference voltage is directly added into the D/A converter output.

In the automotive industry electronic circuits are used to realize large systems with more functions. However, the automotive environment is very extreme, and the temperature variations can be in the range of –15°C to 105°C. A supply voltage regulator handles the stabilization of the supply voltage in the car, and the reference for this regulator must be able to withstand the extreme automotive environment [3]. Similarly, in battery-operated DRAMs, voltage references are used for power-supply voltage stabilization. In this case, the power consumption is of prime importance.

Bandgap voltage references (BGRs) are still the most popular precise reference used in various circuits [1, 2]. A bandgap voltage reference has high power supply noise rejection, and its output voltage is very stable against temperature and process variations. It can be implemented using available vertical or lateral BJTs in any standard CMOS technology [4], [5]. However, when the supply voltage is close to 1 V, the performance of a conventional bandgap reference degrades and the design problems accumulate [6]. As an alternative, voltage references can also be implemented in MOS technology using the threshold voltage difference [7]. But this solution requires transistors with different thresholds that were available, up to the recent time, in NMOS and SOI technologies only. The difference between the absolute values of threshold voltages existing in initial versions of standard CMOS technologies was also used [8].

Yet, in the modern standard low-cost technologies, the so-called regular n- and p-channel transistors have the threshold voltages nearly of the same values. But these technologies include new devices, first of all, "native" or "natural" transistors. In addition, these technologies include the transistors with a threshold voltage that is about half of the corresponding regular transistor threshold voltage. The application of these transistors for the design of sub-1 V voltage references has not yet been investigated. We develop the circuits for implementing voltage references using these devices, and investigate their behavior over the range of temperatures from –25°C to 125°C.

1.2 Thesis outline and contributions

To successfully design a CMOS current/voltage reference, one must have a thorough understanding of the temperature behavior of bipolar and MOS transistors. Therefore, in Chapter 2 we review the theory and the issues with respect to temperature that surround the design of different groups of voltage references. We review the temperature dependence of the transistor base-emitter voltage V_{BE} and describe the assumptions concerning the temperature dependence of some basic semiconductor physical properties (energy bandgap, intrinsic carrier concentration) accepted in the analysis. Then we describe the temperature behavior of the difference of two base-emitter voltages. At last, we discuss the very important dependence that results in the voltage proportional to the thermal voltage. The knowledge of basic dependencies is necessary for the design of classical bandgap references.

The following is the description of the temperature dependence of the MOS transistor threshold voltage, and the temperature dependence of carrier mobility. The equations that are generally used to describe the temperature behavior of the CMOS threshold voltage and mobility are presented. Special attention is given to existence of the zero temperature coefficient (ZTC) point. This point is present in all modern MOS technologies. The presence of the zero temperature coefficient point in the transconductance characteristics of a CMOS transistor is studied, and the conditions under which such a point can exist are investigated. This fact was used for design and investigation of a number of non-bandgap references developed in this department.

Historically, the first voltage references were the bandgap voltage references. They are the most precise references, yet require the highest power supply voltage. These references compensate the base-emitter or diode voltage temperature dependence by that of the thermal voltage. In Chapter 3 we review the techniques used for the design of these most widely used voltage references. Their development in bipolar technology and adaptation of these references to new conditions, namely the realization in BiCMOS and CMOS technologies, is shown, and realization under the conditions of reduced power supply voltage is discussed.

To get a clear insight, first we have to study the basic function of bandgap references, including a general description of the temperature compensation. Then, as the basic structure is found, the techniques used for the design of first-order bandgap references will be studied. Also, the methods used for the design of low-voltage BGR are studied. This review and study goes up to the latest contributions in this particular type of circuits.

Chapter 4 describes the basic methods of design of current sources with different temperature dependencies. These current sources are necessary for the bias circuits used in voltage references. In addition, the current sources with the proportional-to-absolute-temperature (PTAT) dependence of the output current, as well as the current sources with the higher degree ($PTAT^2$, $PTAT^3$, etc.) of this dependence are necessary for the design of the curvature-compensated bandgaps, and, in the future, some non-bandgap references.

Chapter 5 gives a brief review of the basic ideas used in the design of curvature-compensated bandgap references. Some special structures, such as quadratic law temperature compensation, second-order curvature-compensated reference, and high-order temperature compensation will be given. This branch of references is continuing to grow.

The unsatisfactory performance of the traditional bandgap voltage references under the conditions of reduced (below 1 V) power supply voltage forced the designers to search for other compensation mechanisms that would be suitable for voltage reference realization, especially in the new sub-micron CMOS technologies.

Chapter 6 describes the recent work on non-bandgap voltage references using the mutual compensation of carrier mobility and threshold voltage temperature effects. The application of this mechanism to design of voltage references was started in this department. Chapter 6 summarizes the results obtained for this type of references. It describes some interesting solutions and the results of their simulation and experimental investigation. The dependence of the designs on some specific properties of used technologies, and the necessity of tuning forced us to investigate other possibilities.

In Chapter 7 we develop and investigate voltage references based on the threshold-voltage-difference architecture that can be realized in modern standard CMOS technologies. Three types of voltage references are investigated. In the first type the gate-source voltages of two transistors having different threshold voltage values is applied to a resistor. If the transistor parameters are chosen in a specific way, the current developed in this resistor will be defined by the difference of threshold voltage values. Using a current mirror one can obtain the circuit output voltage that is proportional to this difference. This difference is very stable with temperature and may be used as a reference voltage.

The second type of reference voltage circuit investigated in this chapter does not need any resistors. The output voltage of this circuit is also defined by the difference of two threshold voltages. It is shown that this voltage reference may operate at very low currents.

Both types of considered voltage references allow us to design for power supply voltages as low as 0.6 V.

The third type of reference uses an asymmetric differential amplifier with one grounded input and 100% feedback from the amplifier output to the second input. The importance of this reference is that it indicates that, for the reference voltages for low power supply voltages, the problems of designing a temperature independent current source and voltage reference are equivalent.

Chapter 8 is dedicated to the design of the voltage references considered in Chapter 7, and provides layouts and packaging information. Unfortunately, the limitations imposed by CMC for the university multi-project chips did not allow us to realize the best circuits from the references described in the previous chapter. We were able to realize the references using regular n-channel transistors and the so-called "native" or "natural" n-channel transistors. The realized designs allow us to verify only the basic ideas of the approach chosen in this thesis. The experimental investigation of the fabricated in 0.18-micron CMOS technology voltage references will be given in this chapter as well if the circuits will arrive before the thesis completion. At the time of

writing two reference circuits have been submitted to CMC for fabrication and the chips will arrive in January 2006 by CMC schedule.

The Summary and Conclusions chapter summarizes the experience obtained in the investigation of the proposed class of voltage references, and outlines directions for future work.

Chapter 2 Basic Temperature Dependencies

In this chapter we consider some basic temperature dependencies of transistor parameters. First of all, we consider the temperature dependence of the base-emitter voltage V_{BE} of the bipolar transistor biased by collector currents with different temperature dependencies. The obtained expression and its approximation are necessary in the design of simple bandgap references and the curvature-compensated bandgap references. This is followed by a discussion of threshold voltage temperature dependency. The linearity of this dependency is one of the main assumptions used in the design of the voltage reference proposed in Chapters 6 and 7. Then the conditions for the existence of the zero-temperature-coefficient (ZTC) point in the MOS transistor transconductance characteristics are investigated. These results are important for understanding the operation of some previously designed nonbandgap voltage references.

2.1 Temperature dependence of the base-emitter voltage

The collector current of an n-p-n bipolar transistor exhibits an exponential relationship to the base-emitter voltage [9], and is expressed as

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \tag{2-1}$$

where I_C is the collector current, I_S is the saturation current in the forward-active region, V_{BE} is the base-emitter (diode) voltage, and $V_T = kT/q$ is the thermal voltage (approximately 26 mV at room temperature). From (2-1) one derives that V_{BE} is

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \tag{2-2}$$

The saturation current I_S is defined [9] by the electron charge $q = 1.6 \cdot 10^{-19}$ Coulomb, the intrinsic carrier concentration n_i (approximately $1.5 \cdot 10^{10}$ cm^3 for silicon), the dif-

fusion constant for electrons D_n, the emitter cross-sectional area A_E, the effective width of the base region W_B, and the base doping density N_A. For a transistor of parallelepiped shape this current is

$$I_S = \frac{qn_i^2 D_n A_E}{W_B N_A} \tag{2-3}$$

In a real transistor only a central part may be approximated as a parallelepiped. Yet, if one uses Q_B, the number of doping atoms in the base per unit of average effective area $\overline{A}_E$ of the emitter, and $\overline{D}_n$, the average value of the electron diffusion constant in the base, then one can write

$$I_S \approx \frac{qn_i^2 \overline{D}_n \overline{A}_E}{Q_B}. \tag{2-4}$$

where $Q_B = W_B N_A$. The temperature dependence of the intrinsic carrier concentration and the average electron diffusion constant can be described by [10]

$$n_i^2 = AT^3 \exp\left(-\frac{V_{g0}}{V_T}\right) \tag{2-5}$$

and

$$\overline{D}_n = V_T \overline{\mu}_n \tag{2-6}$$

respectively, where A is a temperature-independent constant, T is the absolute temperature, V_{g0} is the extrapolated diode voltage at 0°K. In this work we consider that V_{g0} is a temperature-independent constant (in reality it is weakly dependent on temperature [11]). In (2-6) $\overline{\mu}_n$ is the average mobility for the minority carriers in the base,

$$\overline{\mu}_n = BT^{-m} \tag{2-7}$$

where B is a temperature-independent constant. As a first approximation one may assume that m is also a temperature-independent constant (more about it is discussed below). The relationship for the saturation current I_S is more explicitly expressed by substituting (2-5) to (2-7) in (2-4). This results in

$$I_S = \frac{q\left[AT^3 \exp\left(-\frac{V_{g0}}{V_T}\right)\right](V_T B T^{-m})\bar{A}_E}{Q_B} = CT^{(4-m)} \exp\left(-\frac{V_{g0}}{V_T}\right) \qquad (2\text{-}8)$$

where C is a temperature-independent constant defined by all the constants in the left part of equation (2-8) such as q, A, B, $\bar{A}_E$, Q_B and k/q, where $k = 8.62 \cdot 10^{-5}$ eV/°K. Finally, the collector current will be assumed to have a temperature dependence whose behavior is described by

$$I_C = DT^x \qquad (2\text{-}9)$$

where D is a constant and x is an arbitrary number (chosen by the design engineer) defined by the temperature dependence of the bias current forced through the collector. In practice the most frequently used values are $x = 0$, i.e. a temperature-independent current, and $x = 1$, i.e. a proportional-to-absolute temperature (PTAT) current. Consequently, the temperature dependence of the base-emitter voltage can be rewritten as

$$V_{BE} = V_T \ln\left[\frac{D}{C} T^{[x-(4-m)]} \exp\left(\frac{V_{g0}}{V_T}\right)\right] = V_{g0} + V_T \ln\left(\frac{D}{C}\right) - [(4-m)-x]V_T \ln T \qquad (2\text{-}10)$$

However, a more appropriate form of the base-emitter relationship, for the purpose of design, is its temperature dependence as a function of the reference temperature, T_r (usually 300 °K). This form can be derived by using the relationship (2-10) at the reference temperature

$$V_{BE}(T_r) = V_{g0} + V_{T_r} \ln\left(\frac{D}{C}\right) - [(4-m)-x]V_{T_r} \ln T_r \qquad (2\text{-}11)$$

and eliminating $\ln(D/C)$ from (2-10) and (2-11). This gives

$$V_{BE} = V_{g0} - \frac{T}{T_r}[V_{g0} - V_{BE}(T_r)] - [(4-m)-x]V_T \ln\left(\frac{T}{T_r}\right) \qquad (2\text{-}12)$$

Equation (2-12) shows that the temperature dependence of V_{BE} includes three terms. The expression including first two terms

$$V_{BE} \approx V_{g0} - \frac{T}{T_r}[V_{g0} - V_{BE}(T_r)] \qquad (2\text{-}13)$$

is used as a first approximation in the design of the so-called non-curvature compensated bandgap references. One can also see that if

$$x = 4 - m \tag{2-14}$$

then the last nonlinear term of (2-12) disappears. As was mentioned above, the most frequently used case is $x = 1$. This choice diminishes the nonlinear term but does not eliminate it completely. In modern technologies m is in the range of 0.5 to 2. The design and use (to bias the current sources) of x in the range from 2 to 3.5 produces the so-called curvature-compensated references. These opportunities will be reviewed in the next chapters.

2.2 Temperature dependence of the difference of two base-emitter voltages

Let us consider now (Figure 2.1(a)) the temperature dependence of the difference of two emitter-base voltages. We assume that the bias currents for transistors Q_1 and Q_2 are matched, i.e.

$$I_{C1} = I_{C2} = I_C \tag{2-15}$$

Then, assuming that these transistors are fabricated in the same technology, it follows from (2-2) and (2-4), that

$$V_{PTAT} = V_T \ln(I_{S1} / I_{S2}) = V_T \ln(\overline{A}_{E2} / \overline{A}_{E1}) \tag{2-16}$$

In many practical circuits transistor Q_2 is realized as the parallel connection of N transistors similar to Q_1 (Figure 2.1(b)) and the base current is neglected. In this case $\ln(\overline{A}_{E2} / \overline{A}_{E1}) = \ln N$ and

$$V_{PTAT} = V_T \ln N = (kT / q) \ln N \tag{2-17}$$

Thus, the circuit of Figure 2.1(b) generates a voltage proportional to the absolute temperature (PTAT). It is the most universal circuit for the generation of this type of voltage. Unfortunately, the realization of this circuit requires that the power supply voltage V_{DD} be higher than $V_{BE} \approx 0.7$ V (practically, about 0.9 V). The lack of circuits

generating a PTAT voltage with the power supply less than 0.7 V is the main obstacle to the design of precise references operating with low-voltage power supplies.

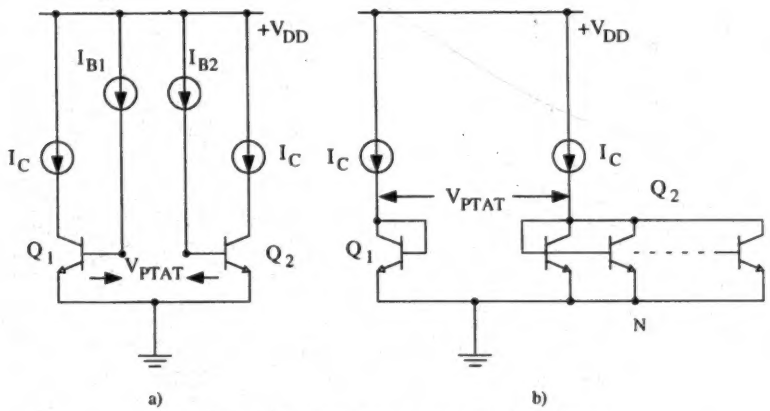

Figure 2.1 Generation of the PTAT voltage

2.3 Threshold voltage temperature dependence

A commonly used [12] expression for the threshold voltage of a MOS transistor is

$$V_{TH} = \phi_{ms} \pm \frac{Q_{ss}}{C_{ox}} + 2\phi_F + \Delta V_T(N_i, d_i) \pm \gamma(N_s, t_{ox}, L, W)\sqrt{2\phi_F + V_0 + |V_{SB}|} \qquad (2\text{-}18)$$

where the positive or negative sign refers to n-channel or p-channel devices, respectively. In equation (2-18) ϕ_{ms} is the metal-silicon (or gate-semiconductor) work function difference, Q_{ss} is the surface-state charge density per unit area, C_{ox} is the gate oxide capacitance per unit area, ϕ_F is the Fermi potential of the substrate, $\Delta V_T(N_i, d_i)$ is the threshold shift owing to a channel implant N_i with depth, d_i, and γ is the body-effect constant that depends on the substrate doping N_s, the gate oxide thickness t_{ox}, and the channel length L and width W. Finally, $V_0(N_s, N_i, d_i)$ denotes a correction term related to the threshold shift implant. For enhancement devices with a ΔV_T shifting implant of the same type as the substrate, V_0 has a sign opposite to that of ϕ_F.

The major contributors to the variation of the threshold voltage with temperature are the Fermi potential ϕ_F, and the gate-semiconductor work function difference ϕ_{ms}. The Fermi potential is expressed [13] by

$$\phi_F(T) = \pm\frac{kT}{q}\ln\left(\frac{n_c}{n_i(T)}\right) \tag{2-19}$$

where n_c is the carrier concentration and n_i is the intrinsic carrier concentration (its temperature dependence is given by (2-5)). When impurity atoms are added, at relatively elevated temperature most donors and acceptors are ionized, and the carrier concentration n_c can be expressed [14] by

$$n_c = \begin{cases} \frac{1}{2}\left[(N_D - N_A) + \sqrt{(N_A - N_D)^2 + 4n_i^2}\right] & (n\text{-}type) \\ \frac{1}{2}\left[(N_A - N_D) + \sqrt{(N_D - N_A)^2 + 4n_i^2}\right] & (p\text{-}type) \end{cases} \tag{2-20}$$

where N_D and N_A are donor and acceptor concentrations, respectively. As long as the magnitude of the net impurity concentration $|N_D - N_A|$ is much larger than n_i (this condition is usually satisfied over a wide temperature range known as the extrinsic region) then

$$n_c = \begin{cases} N_D & (n\text{-}type) \\ N_A & (p\text{-}type) \end{cases} \tag{2-21}$$

For a silicon gate doped oppositely to the substrate, the contact potential is essentially determined by the p-n product. Therefore, for an n-type doped gate, the gate-semiconductor work function is expressed [15] as

$$\phi_{ms}(T) = \begin{cases} -\frac{kT}{q}\ln\left(\frac{N_s N_p}{n_i^2}\right) & (NMOS) \\ -\frac{kT}{q}\ln\left(\frac{N_s}{N_p}\right) & (PMOS) \end{cases} \tag{2-22}$$

where N_p is the carrier concentration in the polysilicon gate.

Differentiating equation (2-18) with respect to the temperature and considering the fact that ϕ_{ms} and ϕ_F are the major factors which cause the threshold voltage temperature dependence, the value of α_{VT} will be equal to

$$|\alpha_{VT}| = \left|\frac{\partial V_{TH}}{\partial T}\right| = \left|\frac{\partial \phi_{ms}}{\partial T} + 2\frac{\partial \phi_F}{\partial T} + \frac{\gamma}{\sqrt{2\phi_F + V_0 + |V_{SB}|}}\frac{\partial \phi_F}{\partial T}\right| \quad (2\text{-}23)$$

Taking into consideration (2-5) and (2-22) one finds that for an n-doped gate

$$\frac{\partial \phi_{ms}}{\partial T} = \frac{1}{T}\left(\phi_{ms} + V_{g0} + \frac{3kT}{q}\right) \quad (2\text{-}24)$$

Using (2-19), the temperature coefficient of ϕ_F is given by

$$\frac{\partial \phi_F}{\partial T} = \frac{1}{T}\left(\phi_F - (\frac{V_{g0}}{2} + \frac{3kT}{2q})\right) \quad (2\text{-}25)$$

Therefore, the temperature coefficient of the threshold voltage becomes

$$|\alpha_{VT}| = \left|\frac{\partial V_{TH}}{\partial T}\right| = \left|\frac{\phi_{ms}}{T} + 2\frac{\phi_F}{T} + \frac{\gamma(N_s, t_{ox}, L, W)}{\sqrt{2\phi_F + V_0 + |V_{SB}|}}\right| \quad (2\text{-}26)$$

The derivation shows that (2-24) is a weak function of temperature in the practical range 200-400°K. In this range the threshold voltage decreases approximately linearly [15] with an increase in temperature. The following equation is usually used

$$V_{TH}(T) = V_{TH}(T_0) + \alpha_{VT}(T - T_0) \quad (2\text{-}27)$$

where α_{VT} has a negative value and may be considered as approximately constant. The value of α_{VT} depends on the process and varies [10, 16] from -1 mV/°C to - 4 mV/°C. In modern CMOS processes this figure is close to –0.8 mV/°C [17].

Although the value of α_{VT} is assumed to be constant, there are a number of factors [12] that affect its value. As equation (2-23) shows, the value of $|\alpha_{VT}|$ depends on the value of $|V_{SB}|$. A higher back bias $|V_{SB}|$ causes a smaller magnitude of $|\alpha_{VT}|$. The length of the transistor channel also affects $|\alpha_{VT}|$. For a short-channel transistor, $|\alpha_{VT}|$ is smaller due to the fact that part of the depletion charge associated with channel formation is depleted from the source and drain rather than from the gate [13].

This effect leads to a reduction of the body effect γ that will cause $|\alpha_{VT}|$ to decrease. The width of the device also influences the device behavior [13]: a narrow device has an increased value of γ, and, hence, an increased value of $|\alpha_{VT}|$. Both of these effects can be reduced making the device big and wide, for example, by making the length and width ten times larger than the smallest length of the gate. For example, $|\alpha_{VT}|$ may be considered as independent on L and W for a device in 0.18-μm CMOS technology if L and W are larger than 2 μm each [18].

2.4 Compensation of threshold voltage and mobility temperature effects

Mutual compensation of mobility and threshold voltage temperature effects in field-effect transistors is well known [19, 20]. The detailed investigation of this compensation resulting in the presence of the common or zero temperature coefficients (ZTC) point in MOS transconductance characteristics (Figure 2.2) was done in [17]. In early MOS technologies this ZTC point was observed for high gate-source voltages [20] that exceed the power supply voltages of modern circuits and this fact may explain that the compensation has not obtained proper attention. Yet, the exact behavior of transistor transconductance characteristics in the vicinity of ZTC bias point is important for the design of circuits operating over a wide temperature range [21-24], and, also (Chapter 6), may be used for the design of some voltage references.

The ZTC point exists for a series of industrial CMOS technologies [25]. It was also shown [25] that, using an external constant current source for the biasing, a diode-connected MOS transistor at the ZTC point produces a temperature-stable voltage (the reported stability was 13 ppm/°C over the range of 0-125 °C)

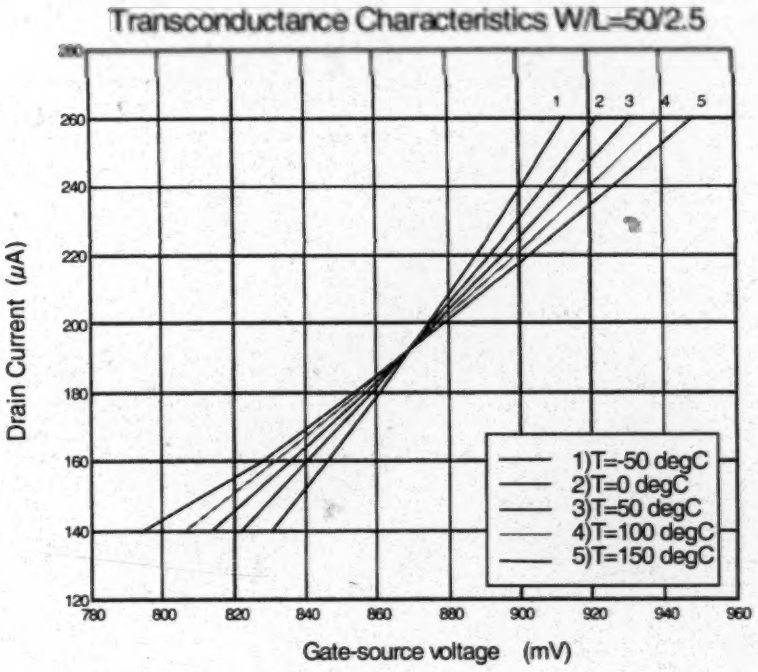

Figure 2.2 Transconductance characteristics in the vicinity of the ZTC point

2.4.1 Conditions for compensation

Following [26] one writes the n-channel transistor drain current equation as

$$I_d = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{gs} - V_{TH})^2 \tag{2-28}$$

Both the carrier mobility μ_n and the threshold voltage V_{TH} change with temperature. For a given temperature T_1, one can find the bias voltage

$$V_{GS} = V_{TH}(T_1) + [2\mu_n \frac{\partial V_{TH}/\partial T}{\partial \mu_n / \partial T}]|_{T=T_1} \tag{2-29}$$

such that the drain current I_d at T_1, satisfies the condition $(\partial I_d)/(\partial T)|_{T=T_1} = 0$. The voltage V_{TH} changes as in (2-27), where T_0 denotes the reference temperature, and $\partial V_{TH}/\partial T = \alpha_{VT}$ is a negative constant. The mobility depends on temperature as [16]

$$\mu_n(T) = \mu_n(T_0)(T/T_0)^{\alpha_\mu} \tag{2-30}$$

Let us assume, for now, that α_μ is a constant. When (2-30) and (2-27) are substituted in (2-29) one determines that the required bias voltage is

$$V_{GS} = V_{TH}(T_0) + \alpha_{VT}T_1(1+\frac{2}{\alpha_\mu}) - \alpha_{VT}T_0 \tag{2-31}$$

If, in addition, $\alpha_\mu = -m = -2$ (compare with 2-7), then there also exists a temperature-independent voltage

$$V_{GS} = V_{GSF} = V_{TH}(T_0) - \alpha_{VT}T_0 \tag{2-32}$$

that biases the transistor to a temperature-independent drain current I_{DF}. If (2-32) and (2-27) are substituted into (2-25), then one obtains

$$I_D = \frac{\mu_n(T)C_{ox}}{2}\left(\frac{W}{L}\right)(\alpha_{VT}T)^2 \tag{2-33}$$

If the temperature dependence (2-30) is substituted into (2-33) with $\alpha_\mu = -m = -2$ one obtains

$$I_D = I_{DF} = \frac{\mu_n(T_0)T_0^{\,2}C_{ox}}{2}\left(\frac{W}{L}\right)\alpha_{VT}^{\,2} \tag{2-34}$$

In this case the temperature decrease of mobility exactly compensates for the temperature decrease of the threshold voltage, and the transistor biased by the voltage V_{GSF} has a temperature-independent drain current I_{DF}.

A diode-connected transistor can be biased by an independent current source. Rewriting (2-25) as

$$V_{gs} = V_{TH} + \sqrt{\frac{2I_d}{\mu_n C_{ox}(W/L)}} \tag{2-35}$$

one can find, for a given temperature T_2, the drain current I_d that provides the condition $(\partial I_d)/(\partial T)|_{T=T_2} = 0$. For this current the voltage V_{gs} becomes equal to

$$V_{GS} = V_{TH}(T_0) + \alpha_{VT}T_2(1+\frac{2}{\alpha_\mu}) - \alpha_{VT}T_0 = V_{GSF} + \alpha_{VT}T_2\left(1+\frac{2}{\alpha_\mu}\right) \tag{2-36}$$

When $\alpha_\mu = -m = -2$, this voltage has the same value as in (2-32), and the required I_D is given by (2-34).

Hence, if this point (V_{GSF}, I_{DF}) exists, and the transistor transconductance characteristics obtained at different temperatures have a common intercept point, then one can assume that in this technology $\alpha_\mu = -m \approx -2$. This is important in the design of higher-order bandgap references.

2.4.2 The transconductance characteristics in the vicinity of the ZTC point

For $V_{gs} = V_{GSF} + \Delta V_{GS}$, and an arbitrary temperature T where $V_{gs} - V_{TH} = \Delta V_{GS} - \alpha_{VT} T$, the drain current becomes

$$I_d = \frac{\mu_n(T_0)(T/T_0)^{-2} C_{ox}}{2}\left(\frac{W}{L}\right)(\Delta V_{GS} - \alpha_{VT} T)^2 \approx I_{DF}\left(1 - \frac{2}{\alpha_{VT} T}\Delta V_{GS}\right) \qquad (2\text{-}37)$$

The simulated transconductance characteristics (with T as a parameter) shown in Figure 2.2 confirm this. They are for an n-channel device in 0.35μm CMOS technology. They have a common intercept point ($V_{GSF} \approx 869$ mV, $I_{DF} \approx 192$ μA), and, indeed, can be approximated as pieces of straight lines with a slope that is inversely proportional to temperature. This linear dependence, as we will see in Chapter 6, is essential for the design of some voltage references.

If $\alpha_\mu \neq -2$, the point (V_{GSF}, I_{DF}) does not exist. Then, for $V_{gs} = V_{GSF} + \Delta V_{GS}$, the drain current becomes

$$\begin{aligned} I_d &= \frac{\mu_n(T_0)(T/T_0)^{\alpha_\mu} C_{ox}}{2}\left(\frac{W}{L}\right)\left(\Delta V_{GS} + \frac{2\alpha_{VT} T}{\alpha_\mu}\right)^2 \\ &\approx I_{DF}\left(\frac{2}{\alpha_\mu}\right)^2\left(\frac{T}{T_0}\right)^{2+\alpha_\mu}\left(1 + \frac{\alpha_\mu}{\alpha_{VT} T}\Delta V_{GS}\right) \end{aligned} \qquad (2\text{-}38)$$

The characteristics are again pieces of straight lines with a slope that is inversely proportional to the temperature. Yet, they do not have a common intercept point, they

have a "bottleneck" only (in reality, one has always a "bottleneck", not a point). The initial point of each characteristic (obtained for $\Delta V_{GS} = 0$) depends on temperature. Such characteristics (Figure 2.3) were obtained for p-channel transistors of the same 0.35μm CMOS technology.

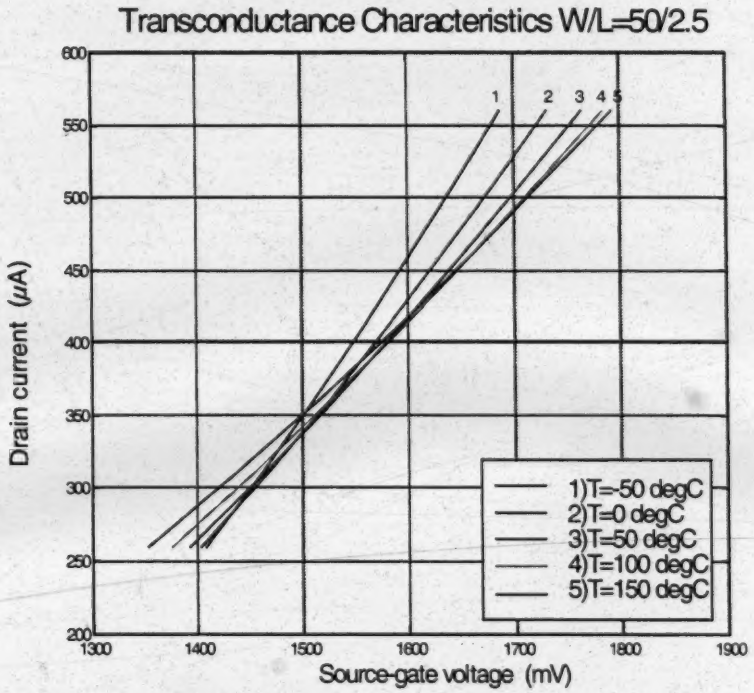

Figure 2.3 Transconductance characteristics of the p-channel transistor

Introducing $\Delta T = T - T_0$ one can approximate $(T/T_0)^{2+\alpha_\mu} \approx 1 + (2+\alpha_\mu)\dfrac{\Delta T}{T_0}$. Then the drain current in the vicinity of the "bottleneck" can be rewritten as

$$I_d \approx I_{DF}\left(\frac{2}{\alpha_\mu}\right)^2\left[1+(2+\alpha_\mu)\frac{\Delta T}{T_0}\right]\left[1+\frac{\alpha_\mu}{\alpha_{VT}}\frac{\Delta V_{GS}}{(T_0+\Delta T)}\right] \qquad (2\text{-}39)$$

When $\alpha_\mu = -2$, the result (2-39) coincides with (2-37).

2.5 Summary

In this chapter, some basic temperature dependencies of transistor parameters were reviewed. The temperature dependence of the base-emitter voltage V_{BE} for bipolar transistors biased by the collector currents with different temperature behavior was found. This dependence was divided into linear and nonlinear parts. This division is important for the design and classification of bandgap voltage references. As we will see later, the approximation using the linear part only is used in the design of the first-order or non-curvature-compensated BGRs. Consideration of the nonlinear part is required in the design of higher-order or curvature-compensated BGRs.

Then the temperature dependence of the threshold voltage V_{TH} was described. This temperature dependence is nonlinear, yet over a relatively wide range of temperatures it can be considered to be linear one, and the temperature coefficient α_{VT} of this dependence may be considered to be a constant. This assumption will be used in the design of non-bangap references.

Finally, we described the conditions when the transconductance characteristics of MOS transistor have a ZTC point. The presence of this point is essential for the design of some non-bandgap voltage references.

Chapter 3 Bandgap First-Order References

This chapter reviews the most popular voltage references, the so-called first order bandgap voltage references. A description of the most important steps in their development will be followed by the basic idea of the design. The techniques, including the most recent one, that are used in the design of these first-order BGRs will be studied.

Any bandgap voltage reference is bipolar in nature. This means that it includes a bipolar transistor (usually in a diode connection), and the temperature-dependent $V_{BE}(T)$ is compensated to obtain a temperature-independent output voltage. If $V_{BE}(T)$ is approximated by the linear dependence (2-13) and the thermal voltage $V_{PTAT} = NV_T = NkT/q$ is used for compensation then one designs a first-order BGR. Only these designs are considered in this chapter. The higher order BGRs, when the full expression (2-12) is considered and the nonlinear term is also compensated, will be considered in Chapter 5.

3.1 Development of the first-order bandgap references

For many years, bandgap references have been used as voltage references in various fields of application, for instance in the automotive industry [27], battery-operated dynamic-random access memories (DRAMs) [28] and many other circuits. A bandgap voltage reference has high power supply noise rejection, and its output voltage is very stable against temperature and process variations.

Many of the bandgap references used in these diverse applications are based on the idea proposed by Hilbiber in 1964 [29]. He proposed to add and subtract several base-emitter voltages with different first-order behaviors for the temperature compensation of a base-emitter voltage. Because of using several base-emitter voltages, the required power supply voltage was very high. In 1965, Widlar found a PTAT voltage that was

proportional to the absolute temperature by using the difference of two junction voltages [30]. In 1971, Widlar used this PTAT voltage for the compensation of the temperature behavior of base-emitter voltage in the design of a bandgap reference [31] that required a lower power supply compared to Hilbiber's proposal. Later, a number of articles describing several designs for the bandgap references appeared [32-35]. Most of the proposed topologies were based on Hilbiber or Widlar proposals or a combination of them. The works [29-35] have established the main ideas in the design of the first-order compensated BGRs. All of these references were designed for a bipolar technology.

Further development of the first-order BGRs is defined by two trends.

First, the bipolar technologies were gradually replaced by CMOS technologies. The first-order BGRs were adapted to these technologies. The compensation bipolar core was preserved using parasitic lateral or vertical bipolar transistors. The signal processing part was redesigned using MOS transistors. Only these designs will be discussed here.

Second, a more profound influence is the tendency to reduce the power supply voltage. If $V_{BE}(T)$ is compensated by putting V_{PTAT} in series with it, the resulting voltage is about 1.25 V close to $V_{g0} \approx 1.215$ V. This voltage is very stable (the typical TCs are from 10 to 20 ppm/°C), and very frequently used as the output voltage of the reference V_{REF} (sometimes, for convenience, the output voltage is trimmed to 1.25 V). The series summation requires that the power supply voltage V_{DD} be about 1.5 V. When the supply voltage is below the bandgap voltage, i.e. below 1.21 V, one has to use an indirect compensation. Usually currents proportional to V_{BE} and V_T are derived and summed [36, 37], and their temperature-dependent components compensate each other. The resulting current is used to create the output voltage across the temperature-independent resistor. This indirect approach reduces the quality of BGRs, and the obtained stability is in the range of 30 to 40 ppm/°C. The required power supply voltages are about 0.9 V (the lowest value which is known to the author [36] is 0.84 V).

The addition of the deep n-well and p-well in triple-well CMOS technologies widened the bipolar capabilities. The parasitic BJTs are exploited in n-well and p-well, and some new designs of compensation core are found [38)]. Yet all these new solutions did not allow us to reduce the power supply voltage to below 0.95 V.

When the power supply voltage is reduced below 0.8 V the principle of the BGR, operation can not be used at all. In this case the designer is forced to use nonbandgap voltage references. These will be considered in Chapters 6 and 7.

3.2 General idea

By definition, a bandgap reference is a voltage reference for which the output voltage is referred to the bandgap energy (or bandgap voltage) of the used semiconductor. As it was discussed in the previous chapter, the bandgap voltage has a weak temperature dependency. Therefore, if the output voltage of this type of reference is referred to the bandgap voltage a true reference is obtained. In the rest of this chapter, it is assumed that the bandgap voltage is constant over the desired temperature range and is equal to V_{g0}, the extrapolated bandgap voltage at 0°K. For realization of a bandgap reference, at least one component must be available of which a port voltage is related to the bandgap voltage. Since the base-emitter voltage of a bipolar transistor is related to the bandgap voltage, the bipolar transistor is the core component of most bandgap references. Bipolar transistors can also be implemented in CMOS technology.

In the previous chapter we found that the temperature dependence of V_{BE} voltage is given by

$$V_{BE} = V_{g0} - \frac{T}{T_r}[V_{g0} - V_{BE}(T_r)] - [(4-m)-x]V_T \ln\left(\frac{T}{T_r}\right) \qquad (3\text{-}1)$$

This equation shows that the temperature dependence of V_{BE} includes three terms. The expression including only the first two terms

$$V_{BE} \approx V_{g0} - \frac{T}{T_r}[V_{g0} - V_{BE}(T_r)] \qquad (3\text{-}2)$$

is used as approximation in design of first-order BGRs (sometimes they are called non-curvature compensated BGRs) . If we introduce

$$T = T_r + \Delta T \tag{3-3}$$

then equation (3-2) can be rewritten as

$$V_{BE} = a_0 + a_1 \frac{\Delta T}{T_r} + a_2 \left(\frac{\Delta T}{T_r} \right)^2 + a_3 \left(\frac{\Delta T}{T_r} \right)^3 + \ldots + a_n \left(\frac{\Delta T}{T_r} \right)^n + O\left[\left(\frac{\Delta T}{T_r} \right)^{n+1} \right] \tag{3-4}$$

where

$$a_0 = V_{BE}(T_r) \tag{3-5}$$

and the coefficients a_1, a_2, a_3, ... of the Taylor series for $V_{BE}(\Delta T / T_r)$ are defined by the expansion of the term $-[(4-m)-x]V_T \ln(T/T_r)$. Even though the approximation (3-2) shows that the temperature dependence $V_{BE}(T)$ is linear, the coefficient

$$a_1 = -[V_{g0} - V_{BE}(T_r)] - [(4-m)-x]V_T(T_r) \approx -[V_{g0} - V_{BE}(T_r)] \tag{3-6}$$

in its full form shows that even the non-curvature compensated bandgap reference needs tuning because the exact value of the parameter m is not known. Yet, usually $T_r = 300\,^{o}\text{K}$, and the approximation of a_1 given by the right part of (3-6) is sufficient for design of these references.

The thermal voltage $V_T = kT/q$ has a positive temperature coefficient equal to $k/q = 0.086$ mV/^{o}K, and can be used for the first-order compensation of the temperature dependence of base-emitter voltage in the design of BGRs. Assuming that the voltage V_T can be amplified

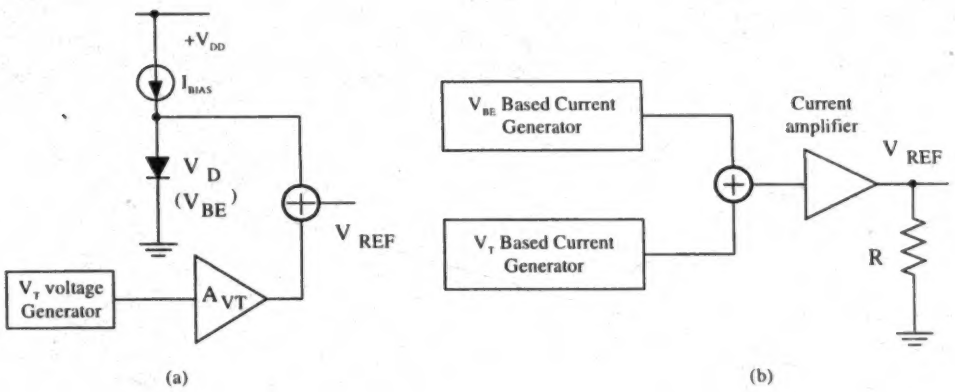

Figure 3.1 Two conceptual implementations of the first-order bandgap reference

by an amplifier with a gain of A_{VT} (Figure 3.1(a)), and summed with the V_{BE} voltage given by (3-2), the resulting voltage will be

$$V_{REF} = V_{BE} + A_{VT}V_T \approx V_{g0} - \frac{T}{T_r}[V_{g0} - V_{BE}(T_r)] + A_{VT}V_T = V_{g0} \tag{3-7}$$

Rearranging the terms we find that the required coefficient is

$$A_{VT} = \frac{V_{g0} - V_{BE}(T_r)}{V_T(T_r)} \tag{3-8}$$

For the frequently used values of $V_{go} = 1.215$ V, $V_{BE}(T_r) = 0.65$ V, and $V_T(T_r) = 25.6$ mV one can find that $A_{VT} = 22$.

3.3 Implementations

Most of the first-order bandgap references are implemented using one of the two techniques shown in Figure 3.1. The first techniques directly implement equation (3-7), i.e. two voltages, V_{BE} and $A_{VT}V_T$ are summed in order to obtain a temperature-independent voltage V_{g0}. In the second method (Figure 3.1(b)) two currents, one proportional to V_{BE} and another one proportional to V_T are properly scaled and summed up. The summed current, which is temperature-independent, will go through a resistor

(which is assumed to be temperature-independent), generating a temperature-independent voltage. The second configuration is also known as current-mode (CM) bandgap voltage reference [39], and it is used to design the references with the power supply voltage below 1 V.

To generate a voltage proportional to V_T, the base-emitter voltage difference of two bipolar transistors can be used. Using equation (2-2)

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \tag{3-9}$$

repeated here for convenience, one can find that the base-emitter voltage difference of two BJT transistors with two different emitter areas can be written as

$$\Delta V_{BE} = V_{BE1}(T) - V_{BE2}(T) = \frac{kT}{q}\ln\left(\frac{I_{C1}}{A_{E1}J_s(T)}\frac{A_{E2}J_s(T)}{I_{C2}}\right) = \frac{kT}{q}\ln\left(\frac{I_{C1}}{A_{E1}}\frac{A_{E2}}{I_{C2}}\right) \tag{3-10}$$

where $J_s(T) = I_{s1}(T)/A_{E1} = I_{s2}(T)/A_{E2}$ is the saturation current density, and A_{E1}, A_{E2} are the emitter areas (we omitted the vinculum for convenience).

Figure 3.2 shows the implementation of the bandgap reference using the voltage summation technique. The circuit operates as follows. Transistors M_3 and M_4 form a current mirror that defines the ratio between the emitters in Q_1 and Q_2 (normally the mirror factor is 1). The operational amplifier and the associated feedback loop drive the voltages of nodes 1 and 2 to a value equal to V_{EB2}. Thus the voltage drop across the resistor R_1 is equal to the base-emitter voltage difference of transistors Q_1 and Q_2. Current I_1 is given by

$$I_1 = \frac{\Delta V_{EB}}{R_1} = \frac{V_T}{R_1}\ln\left(\frac{I_2}{A_{E2}}\frac{A_{E1}}{I_1}\right) \tag{3-11}$$

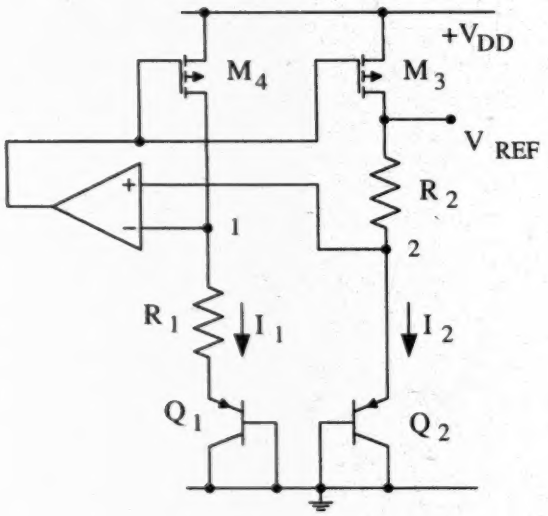

Figure 3.2 CMOS bandgap reference based on voltage summing

where A_{E1} and A_{E2} are the emitter areas of transistors Q_1 and Q_2 respectively. The output voltage, V_{REF} is given by

$$V_{REF} = R_2 I_2 + V_{EB2} \tag{3-12}$$

Substituting (3-11) into (3-12), with $I_1 = I_2$, and using the first two terms in (3-4) for the approximation of V_{EB2} (we note that (3-4) was written for n-p-n transistor, and the same result is valid for V_{EB} in p-n-p transistor) V_{REF} can be written as

$$V_{REF} = \frac{R_2}{R_1} V_T \ln\left(\frac{A_{E1}}{A_{E2}}\right) + a_0 + a_1 \frac{\Delta T}{T_r} \tag{3-13}$$

Finally, using (3-3) one determines that

$$V_{REF} = \frac{R_2}{R_1} V_{Tr}\left(1 + \frac{\Delta T}{T_r}\right) \ln\left(\frac{A_{E1}}{A_{E2}}\right) + a_0 + a_1 \frac{\Delta T}{T_r} \tag{3-14}$$

Here $V_{Tr} = V_T(T_r)$. Therefore, for first-order compensation, the resistor ratio R_2 / R_1 and the ratio of the emitter areas, A_{E1} / A_{E2} should satisfy the relationship

$$\frac{R_2}{R_1} V_{Tr} \ln\left(\frac{A_{E1}}{A_{E2}}\right) + a_1 = 0 \qquad (3\text{-}15)$$

where a_1 is given by (3-6). For the initial design iteration one should choose $(R_2 / R_1)\ln(A_{E1} / A_{E2}) \approx 22$.

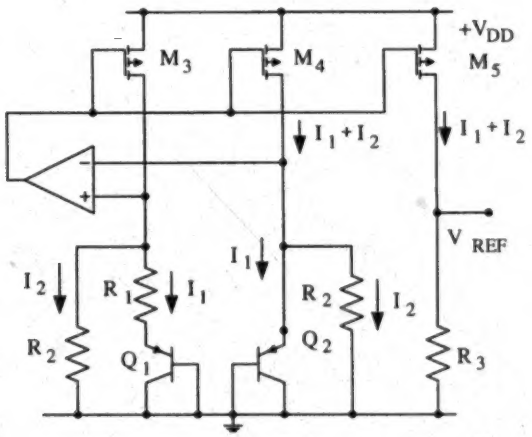

Figure 3.3 CMOS bandgap reference using current processing techniques

Figure 3.3 shows an implementation of a current-mode bandgap reference. Transistors M_3-M_5 form the current mirror with a mirroring factor equal to 1. The operational amplifier drives the voltages of nodes 1 and 2 equal to V_{EB2}. Therefore, the voltage across the resistor R_1 is equal to the emitter-base voltage difference of transistors Q_1 and Q_2, and the current I_1 will be proportional to V_T and is given by

$$I_1 = \frac{V_{EB2} - V_{EB1}}{R_1} = \frac{V_T}{R_1} \ln\left(\frac{A_{E1}}{A_{E2}}\right) \qquad (3\text{-}16)$$

The emitter-base voltage of transistor Q_2, across the resistor R_2, generates current $I_2 = V_{EB2} / R_2$ with negative temperature coefficient. The sum of currents I_1 and I_2 is then equal to

$$I_1 + I_2 = \frac{V_T}{R_1} \ln\left(\frac{A_{E1}}{A_{E2}}\right) + \frac{V_{EB2}}{R_2} \tag{3-17}$$

If the temperature behavior of V_{EB2} is approximated by two terms of the corresponding expansion (3-4) and the condition

$$\frac{V_{Tr}}{R_1} \ln\left(\frac{A_{E1}}{A_{E2}}\right) + \frac{a_1}{R_2} = 0 \tag{3-18}$$

is satisfied, then $I_1 + I_2$ will be temperature-independent to a first approximation. This current is repeated by transistor M_5 and flows through resistor R_3 generating a first-order temperature-compensated voltage V_{REF} which is equal to

$$V_{REF} = V_T \frac{R_3}{R_1} \ln\left(\frac{A_{E1}}{A_{E2}}\right) + \frac{R_3}{R_2} V_{EB2} \tag{3-19}$$

Note that all the resistors should be temperature-matched (i.e. made from the same material) to ensure proper compensation of the output voltage temperature coefficient. As equation (3-19) shows, the circuit can easily achieve a gain or attenuation of the generated bandgap voltage by scaling the value of resistor R_3. This will affect the value of minimum required operating power for the circuit.

The transistors that form the current mirrors in the circuits of Figure 3.2 and Figure 3.3 should operate in the saturation region. Thus, the minimum supply voltage must be maintained in order to prevent the transistors M_3 - M_5 from being forced to operate in the triode region. Therefore, for the circuit of Figure 3.2, the minimum required power supply voltage is expressed by

$$V_{DD\min} = V_{REF} + V_{SDSAT3} \tag{3-20}$$

For this circuit the typical value for V_{REF} is about 1.25 V, and the value of V_{SDSAT3} ranges from 0.1 V to 0.3 V. Thus the theoretical value for the minimum required power supply voltage is about 1.4 V. However, since V_{REF} can be scaled down for the CM voltage reference, the circuit is shown in Figure 3.3 can be designed with a lower power supply voltage compared to the bandgap reference using the voltage summa-

tion. Indeed, the minimum power supply voltage in this case is defined by the branch including transistors Q_2 and M_4, and is equal

$$V_{DD\min} = V_{EB2} + V_{SDSAT4} \tag{3-21}$$

The typical value of V_{EB2} is about 0.65 V. Thus the theoretical value for the minimum required power supply voltage in this case is about 0.85 V.

Offset is one of the main concerns in the design of bandgap references. In the circuits shown in Figure 3.2 and 3.3, the operation of the Op-Amp is to keep the nodes 1 and 2 to an equal value. This is generally true if the gain of the operational amplifier is sufficiently large. However, in real circuits, a possible offset voltage always exists though it can be minimized with suitable Op-Amp design. In both circuits of Figure 3.2 and 3.3, considering that the Op-Amp has the systematic offset voltage V_{OS}, the current I_1 is defined by the condition

$$\Delta V_{EB} + V_{OS} = I_1 R_1 \tag{3-22}$$

If the offset value is comparable to the value of ΔV_{EB}, then the offset will significantly affect the performance of the circuit. One way to reduce the effect of V_{OS} on V_{REF} is to increase the value of ΔV_{EB}. This can be done increasing the ratio A_{E1}/A_{E2}, e.g. replacing one of the transistors by an array of transistors (see Chapter 2).

A very elegant development of the first-order compensated BGRs was proposed recently [38]. This work proposes a simple bandgap reference where a small fraction of V_{BE} in parasitic bipolar transistors and the difference of two V_{BE}'s are combined to generate the reference voltage.

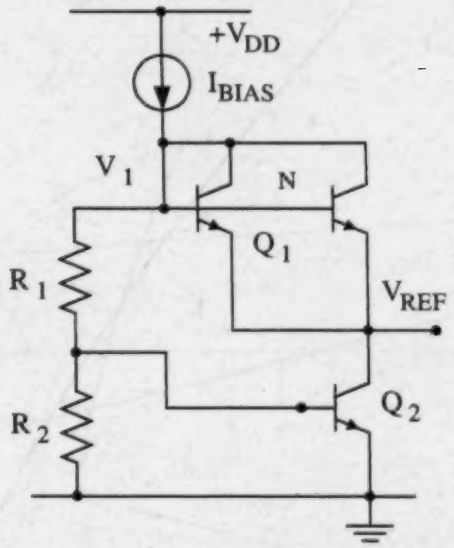

Figure 3.4 Bandgap reference using the circuit of V_{BE} multiplier

Figure 3.4 illustrates the simplified bandgap reference core circuit. The area ratio of n-p-n transistors Q_1 to Q_2 is N. A standard bias circuit [26] generates I_{BIAS}. If the base current of Q_2 is much smaller than the current through R_1 and R_2, then the node voltage V_1 can be approximated as

$$V_1 = V_{BE2} + \frac{R_1}{R_2} V_{BE2} \tag{3-23}$$

Hence, V_1 is proportional to V_{BE2} which, as we know, has a negative temperature coefficient. If V_{BE1} is subtracted from V_1, the reference voltage V_{REF} (coinciding with the collector-emitter voltage V_{CE2}) can be expressed as

$$V_{REF} = V_1 - V_{BE1} = V_{BE2} + \frac{R_1}{R_2} V_{BE2} - V_{BE1} = \Delta V_{BE} + \frac{R_1}{R_2} V_{BE2} \tag{3-24}$$

Transistor Q_1 is diode-connected, and if Q_2 is operating in the forward active region just above saturation, as long as the current gain β of the transistors is sufficiently high, one may write

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_T \ln\left(\frac{\beta+1}{\beta} N\right) \approx V_T \ln N \qquad (3\text{-}25)$$

This circuit may be designed, for example, in triple-well mixed-mode 0.18-μm CMOS technology that includes a deep n-well (as well as an ordinary shallow n-well) layer as part of the process for p-type substrate wafers in order to have individual body potentials for the n-MOS and p-MOS transistors. Then it will be no extra cost to have n-p-n parasitic transistors.

Since the n-p-n transistors are parasitic components, the current gain β can be expected not to be very high. Yet, the experiment shows that the values of β in the range from 8 to 18 can be provided [38]. These values are sufficient to use equation (3-25) and to write that

$$V_{REF} = V_T \ln N + \frac{R_1}{R_2} V_{BE2} \qquad (3\text{-}26)$$

Since the ratio R_1 / R_2 can be chosen to be smaller than one (i.e. one uses a fractional portion of the voltage that is normally necessary in a standard bandgap reference) the transistor ratio N can be made smaller to compensate for the temperature dependence of the second term in (3-26), and the reference voltage V_{REF} is a portion of the normal bandgap reference voltage (which is about 1.2 V). With small R_1 the voltage V_1 is close to $V_{BE2} \approx 0.7$ V, and a bias current source requiring only a voltage drop of 0.2 V can be easily designed. Hence, this reference will be able to operate with the power supply voltages higher than 0.9 V, with 1 V being more than sufficient.

The circuits described so far are designed to compensate for the second term in the expansion (3-4) of the temperature dependence $V_{BE}(T)$. Due to the presence of high-order temperature dependent terms, the output voltage is not constant, and is still weakly dependent on temperature.

3.4 Summary

Voltage references are essential building blocks of many analog and digital circuits. The bandgap reference is the most popular voltage reference used in circuit design. This reference provides an output voltage with low sensitivity to the temperature and process variations. Bandgap references are bipolar in nature but can be implemented in CMOS technologies as well using lateral p-n-p transistors or parasitic vertical bipolar transistors formed with the help of shallow n-well (for vertical p-n-p transistors with grounded collectors) or shallow and deep n-wells (for parasitic vertical n-p-n transistors without restrictions on their collector or emitter potential). In this chapter, the basic principles behind the designs of first-order bandgap references were discussed. These techniques are based on approximation of the V_{BE} temperature dependence by equation (3-2) and using compensation of this temperature dependence by the amplified thermal voltage V_T. With careful design one may reduce the power supply voltage for these references below 1 V, but in practice it is impossible to reduce this voltage below 0.9 V.

The approach does not specify the exact temperature dependence of the bias current in a diode or a transistor. The V_{BE} voltage provides a component (3-2) with negative temperature coefficient, and the term $-[(4-m)-x]V_T(T_r)$ in (3-1) is neglected. Yet, the design of bias currents with different temperature dependencies, first of all with different values of x is important for design of the bandgap references with full or partial compensation of the nonlinear term in (3-1). The design of current references with different dependencies of the current versus temperature is considered in the next chapter.

Chapter 4 Current References

Current references are an essential part of most analog and digital circuits. Amplifiers, phase-locked loops (PLLs) and oscillators are just a few examples of the circuit applications of current references. These circuits are the fundamental building blocks of cellular phones, pagers, laptops and many other consumer electronic products.

The processing of current signals is done faster than the processing of voltage signals, and, therefore, for a given technology, the circuits designed using current-mode approaches operate faster than their voltage-mode counterparts [40]. The current value controls the transconductance of transistors and, in turn, affects the static and dynamic characteristics of circuits. Also, the performance of current sources influences the power consumption, which is an important parameter in many applications.

Often the currents in different parts of a circuit result from mirroring one or more reference currents [2]. It is therefore important to study basic techniques used for the design of current references. Here we consider a particular class of current references, namely, the references producing currents with prescribed temperature dependencies.

We remind here that when the diode or transistor is biased by the temperature-dependent current

$$I_C = DT^x \tag{4-1}$$

the diode or base-emitter voltage of transistor is given by

$$V_{BE} = V_{g0} - \frac{T}{T_r}[V_{g0} - V_{BE}(T_r)] - [(4-m)-x]V_T \ln\left(\frac{T}{T_r}\right) \tag{4-2}$$

The design of first-order bandgap references, as we have seen in the previous chapter, neglects the temperature compensation of the last term in (4-2). The technology parameter m is in the range of 0.5 to 2 (in modern CMOS technologies it is close to 2), and the exact value can be always established by measurements if one is working with a particular process. Then, designing the current references, say, with x = -1, 0, 1, 2, ... and using a combination of currents with different values of x for a diode or

transistor bias current, one can find the combination that results in the minimal influence of the last term.

The most frequently used current references are designed for $x = -1$, $x = 0$, $x = 1$ and $x = 2$. Only these references will be considered in this chapter. The first type ($x = -1$) is called complementary-to-absolute temperature (CTAT) current reference. The second ($x = 0$) produces a temperature-independent current. The third ($x = 1$) generates a proportional-to-absolute temperature (PTAT) current, i.e. a current that is linearly proportional to temperature. Since the PTAT relationship is the most predictable and linear over a wide range of currents, this kind of current reference is the most frequently used one. The CTAT relationship is also rather predictable, and the temperature-independent current references are usually designed combining PTAT and CTAT currents or using available voltage references. Combinations of currents from these three references are often used in conjunction with curvature-correction schemes for the design of precise voltage references (only this part of these applications will be considered in Chapter 5). Square PTAT current ($PTAT^2$) references, or the references with current proportional to the second degree of absolute temperature, require some special circuits, and they appear in the design of curvature-compensated (or second-order compensated) bandgap references only.

The interested reader can find the design of current references for $x = 0.5$, $x = 1.5$, $x =$ and 2.5 in [41].

4.1 PTAT current references

As the name implies, a PTAT current reference generates a current that increases as the temperature increases. Generally, this type of current reference is obtained by forcing a PTAT built-in-voltage across a temperature-independent resistor.

The difference of the base-emitter voltages of two bipolar transistors is proportional to the temperature and can be used for the design of PTAT current references.

The relationship between the base-emitter voltage of an n-p-n transistor and its collector current, as we saw in Chapter 2, is expressed [1] by

$$V_{BE} = V_T \ln\left(\frac{I_C}{J_s A_E}\right) = \frac{kT}{q} \ln\left(\frac{I_C}{J_s A_E}\right) \tag{4-3}$$

where I_C is the collector current, $V_T = kT/q$ is the thermal voltage, J_s is the saturation current density, k is Boltzman's constant, q is the electron charge, A_E is the emitter area, and T is the absolute temperature. Using (4-3), the differences of the base-emitter voltages of two BJT transistors, say, Q_1 and Q_2, can be written as

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{J_s A_{E1}} \frac{J_s A_{E2}}{I_{C2}}\right) = \frac{kT}{q} \ln\left(\frac{I_{C1}}{A_{E1}} \frac{A_{E2}}{I_{C2}}\right) \tag{4-4}$$

where I_{C1} and I_{C2} are the collector currents of transistors Q_1 and Q_2, respectively. Equation (4-4) shows that the difference of two base-emitter voltages is proportional to the absolute temperature.

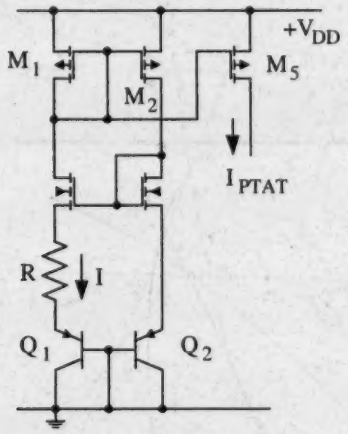

Figure 4.1 PTAT current reference

Figure 4.1 shows a PTAT current reference circuit using the difference of two emitter-base voltages [42]. Transistors M_1 and M_2, form a current mirror developing equal currents for transistors Q_1 and Q_2, i.e. $I_1 = I_2$. Following Kirchhoff's voltage law (KVL) and applying equation (4-4) for p-n-p transistors, one can write

$$I_1 R = V_{EB2} - V_{EB1} = \frac{kT}{q} \ln\left(\frac{I_2}{A_{E2}} \frac{A_{E1}}{I_1}\right) \tag{4-5}$$

The current through M_5 must then be

$$I_{PTAT} = \frac{kT}{qR} \frac{(W/L)_5}{(W/L)_1} \ln n \tag{4-6}$$

where $n = A_{E1} / A_{E2}$ is the emitter-area ratio of Q_1 to Q_2 (A_{E1} is larger than A_{E2}). The advantage of the PTAT current source of Figure 4.1 is that the current generated by this reference is, to a first approximation, independent of the power supply voltage. One drawback of this circuit is that it has an additional stable operating point, which is when I_1 is equal to zero. A start-up circuit is required to prevent the circuit from settling into this state.

In a conventional CMOS process (single n-well technology), the necessary bipolar transistors can be realized using the substrate as part of the transistor. They can be fabricated with the substrate acting as the collector, the well diffusion as the base and the source/drain diffusion as the emitter.

PTAT currents can be also implemented using only CMOS transistors. Figure 4.2 shows one possible completely CMOS design for the implementation of PTAT current generator [1]. The mirror block with mirroring factor of 1, provides equal currents in each branches. Using KVL for the voltage loop consisting of transistors M_1 and M_2 and resistor R, one can write

$$IR = V_{GS1} - V_{GS2} \tag{4-7}$$

The following PTAT current (we show below that this is indeed so), I_{PTAT}, is thus obtained

$$I_{PTAT} = I = \frac{V_{GS1} - V_{GS2}}{R} \tag{4-8}$$

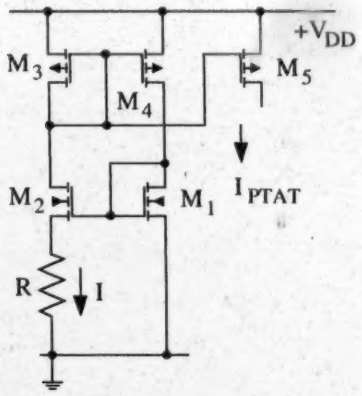

Figure 4.2 CMOS current reference

The MOS transistors, M_1 and M_2, may operate either in the sub-threshold or strong inversion regions (or in saturation in both cases). The generated current can be made proportional to the absolute temperature for both inversion regimes, and we describe the operation of the circuit in these two cases.

4.1.1 Subthreshold region

In the subthreshold region, a MOS transistor operates as a bipolar transistor, and the drain current I_D, of such transistor changes exponentially with variations in V_{GS}, similarly to the bipolar transistor. The voltage V_{GS} of a MOS transistor operating in the subthreshold region is given by [9]

$$V_{GS} = \eta V_T \ln\left(\frac{I_D}{(W/L)I_t}\right) + V_{TH} - \eta V_T \ln\left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \qquad (4\text{-}9)$$

where η and I_t are process-dependent parameters, W and L are the transistor width and length, as usual, and V_{DS} is the drain-source voltage. As soon as V_{DS} voltage exceeds 3-4 values of V_T, one can neglect the last term in (4-9) and write

$$V_{GS} \approx \eta V_T \ln\left(\frac{I_D}{(W/L)I_t}\right) + V_{TH} \qquad (4\text{-}10)$$

Substituting (4-10) into (4-8), the PTAT current is found to be

$$I_{PTAT} = \frac{\eta V_T}{R} \ln\left(\frac{(W/L)_2}{(W/L)_1}\right) \qquad (4\text{-}11)$$

Note that this current is proportional to the absolute temperature, T.

One drawback of this circuit, when M_1 and M_2 are operating in the sub-threshold region, is that the temperature range within which the circuit can operate is limited by the presence of leakage currents. The leakage currents have a positive temperature coefficient, and increase when the temperature increases. Therefore, these currents can override the drain current of the MOS transistor operating in the sub-threshold region at moderately high temperatures [9], and this affects the circuit performance.

4.1.2 Strong inversion region

The same circuit can be used with the transistors operating in strong inversion region. In strong inversion (and in saturation) the V_{GS} of a MOS transistor is expressed as

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}} \qquad (4\text{-}12)$$

Using (4-12) in (4-8) and solving for $I_{PTAT} = I_D$ one finds that [26]

$$I_{PTAT} = I_D = \frac{2}{\mu_n C_{ox} R^2}\left(\frac{1}{\sqrt{(W/L)_1}} - \frac{1}{\sqrt{(W/L)_2}}\right)^2 \qquad (4\text{-}13)$$

We assume that R is a temperature-dependent resistor, and its temperature dependence is expressed as

$$R \approx R_0[1 + \alpha_{R1}(T - T_0)] \qquad (4\text{-}14)$$

where α_{R1} is the first-order temperature coefficient of the resistor and T_0 is the reference temperature. Then, using equation (2-30) from Chapter 2, one can write

$$\mu_n(T) = \mu_n(T_0)(T/T_0)^{\alpha_\mu} \approx \mu_n(T_0)\left[1+\alpha_\mu\left(\frac{T-T_0}{T_0}\right)\right] \tag{4-15}$$

Substituting (4-14) and (4-15) in (4-13) one can find that

$$I_{PTAT} \approx I_{PTAT0}\left[1-\alpha_\mu\left(\frac{T-T_0}{T_0}\right)-2\alpha_{R1}(T-T_0)+2\alpha_\mu\alpha_{R1}\frac{(T-T_0)^2}{T_0}\right] \tag{4-16}$$

where $I_{PTAT0} = \frac{2}{\mu_n(T_0)C_{ox}R_0^2}\left(\frac{1}{\sqrt{(W/L)_1}}-\frac{1}{\sqrt{(W/L)_2}}\right)^2$. Using the first degree approximation for (4-16) one can write that

$$I_{PTAT} \approx I_{PTAT0}[1+\gamma(T-T_0)] \tag{4-17}$$

where $\gamma = -(\alpha_\mu/T_0)-2\alpha_{R1}$. We recall that α_μ is negative, and if $\alpha_{R1} < \frac{|\alpha_\mu|}{2T_0}$ which is usually the case, the coefficient γ will be positive and the circuit of Figure 4.2 is, indeed, a PTAT current generator.

A drawback of this circuit is that it has also an additional operating point similar to the circuit of Figure 4.1. Therefore, a start-up circuit is required to prevent the circuit from getting stuck in this unwanted state.

4.2 CTAT current references

Another useful current reference is a reference that generates a current that is complementary-to-absolute temperature (CTAT). As we will see in Chapter 5, this type of current reference is used in the design of curvature-compensated bandgap voltage references. A simple method to generate a CTAT current is to force a CTAT voltage across a resistor. The base-emitter voltage of a bipolar transistor and the threshold voltage of a CMOS transistor are two voltages that have negative temperature coefficients and thus can be used for generating CTAT currents.

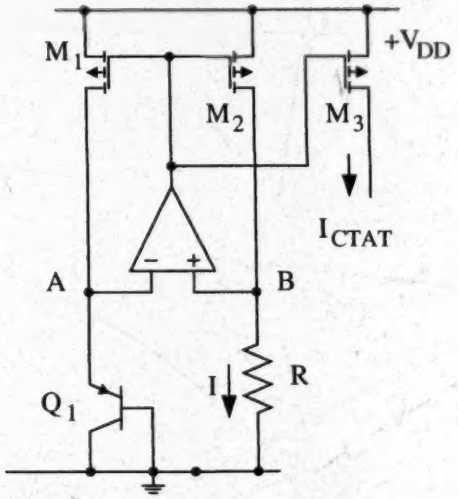

Figure 4.3 CTAT current generator using V_{BE}

Figure 4.3 shows a possible design of CTAT current generator [43] using the base-emitter voltage. The operational amplifier ensures that the voltages at nodes A and B are equal. Therefore, the base-emitter voltage is forced across the resistor, and a CTAT current is generated which is given by

$$I_{CTAT} = \frac{V_{EB}}{R} \tag{4-18}$$

The temperature coefficient of the base-emitter voltage is equal, as we know, to –2.2 mV/°C at room temperature. If the temperature coefficient α_{R1} of the resistor R is positive (which is usually the case), then the current I_{CTAT} will, indeed, show temperature dependence with a negative temperature coefficient.

The threshold voltage of a MOS transistor is another built-in voltage with negative temperature dependence and can be used for the design of CMOS CTAT current references [44]. A possible design for such a circuit is shown in Figure 4.4.

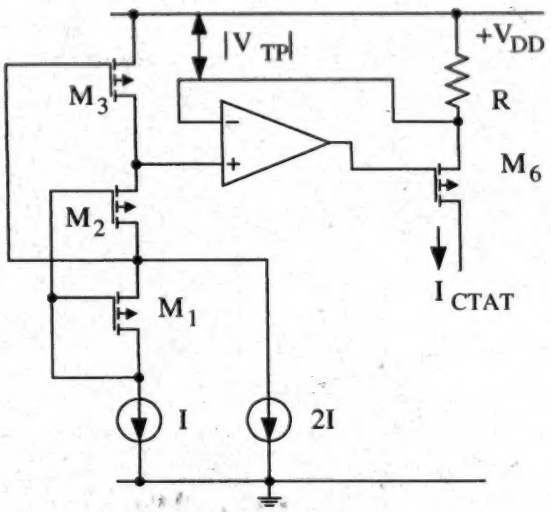

Figure 4.4 CTAT current generator using a $|V_{TP}|$ extractor

The $|V_{TP}|$ threshold extractor can be formed by the transistors from M_1 to M_2 [45]. This voltage is extracted with respect to the V_{DD} line. Assuming the same $|V_{TP}|$ for PFET transistors, one can write the voltage across the drain and source of transistor M_3

$$V_{SD3} = V_{SG3} - V_{SD2} \tag{4-20}$$

One can show that M_1 operates in saturation and M_1 operates in the triode region. Then V_{SD2} is given by

$$V_{SD2} = \sqrt{2I}\left(\sqrt{\frac{1}{K_1}+\frac{3}{K_2}}-\sqrt{\frac{1}{K_1}}\right) \tag{4-21}$$

where $K_i = \mu_p C_{ox}(W/L)_i$, $i = 1, 2, 3$. By making $(W/L)_3$ of M_3 three times that of M_1 and M_2, i.e. $K_1 = K_2 = K_3/3$, and substituting (4-21) in (4-20) one can find that the drain-source voltage of transistor M_3 is expressed as

$$V_{SD3} = |V_{THp}| + \sqrt{\frac{6I}{3K_1}} - \sqrt{\frac{2I}{K_1}+\frac{6I}{K_1}} + \sqrt{\frac{2I}{K_1}} = |V_{THp}| \tag{4-22}$$

This extracted threshold voltage is then buffered and applied to the resistor R to create the I_{CTAT} current that is given by

$$I_{CTAT} = \frac{|V_{THp}|}{R}. \tag{4-23}$$

One disadvantage of this circuit is that since the temperature coefficient of the threshold voltage is somewhat process-dependent, the behavior of the output current will depend on the process as well. The temperature coefficient of the resistor should be positive, and, if possible, small.

4.3 Temperature-independent current references

Temperature-independent current generators are useful for biasing the circuits with fixed current densities across the desired temperature range. They are also used in the design of temperature-independent voltage references. One way to design a temperature-independent current reference is to add PTAT and CTAT currents appropriately. The sum of these currents will give a quasi-temperature-independent current (to a first-order compensation).

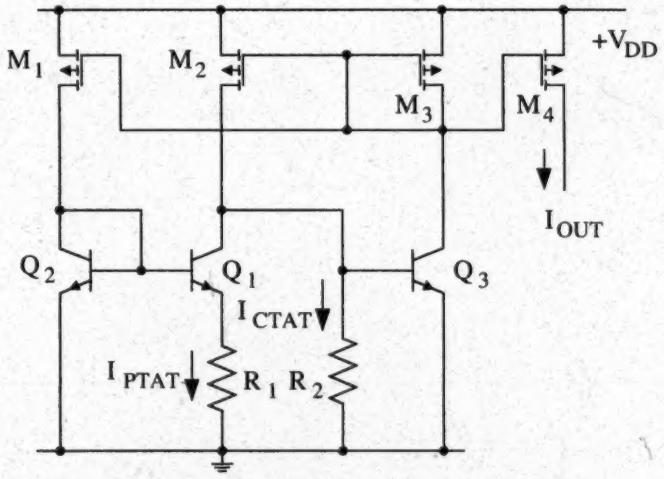

Figure 4.5 The temperature-independent current generator

Figure 4.5 illustrates one possible design [1] based on summing the PTAT and CTAT currents. In this circuit, I_{PTAT} is generated by the loop consisting of transistors Q_1 and Q_2, and resistor R_1. The CTAT current is created by transistor Q_3 and resistor R_2. It is again assumed that the temperature coefficients of the resistors are very low. The PTAT and CTAT currents are then summed, and a temperature-independent current is obtained. The transistors Q_3, M_3 and M_1, Q_2 form a two-stage feedback amplifier keeping the base of Q_1 at the level providing the required summation of currents.

It is interesting to note that the circuit shown in Figure 4.2 can be also used for the design of temperature-independent current generators. In accordance with (4-17), in order to achieve first-order compensation, the first-order temperature coefficient of the resistor should satisfy the following condition

$$\alpha_{R1} = m/(2T_0) \tag{4-24}$$

Using expressions given in [18] it is possible to show that in this current source, one can even achieve second-order compensation by choosing a specific second-order temperature coefficient of the resistor. Unfortunately, the designer is not able usually to choose the resistor temperature coefficients.

The third technique for the design of temperature-independent current references is to force a temperature-independent voltage across a resistor with a very small temperature coefficient. This realization technique requires a temperature-independent voltage reference with second-order temperature compensation. It is more complicated and less frequently used.

4.4 PTAT^2 current references

PTAT^2 current references generate a current that is proportional to the square of the temperature. As we will see in the next chapter, this type of current reference is frequently used in the design of curvature-compensated voltage references. A simple method of implementing a PTAT^2 current reference is to force a PTAT current through a resistor showing CTAT dependence (i.e. having a negative temperature co-

efficient). Such kinds of resistors are quite rare (usually they have a positive temperature coefficient). In addition, the negative temperature coefficients have much wider spread of values.

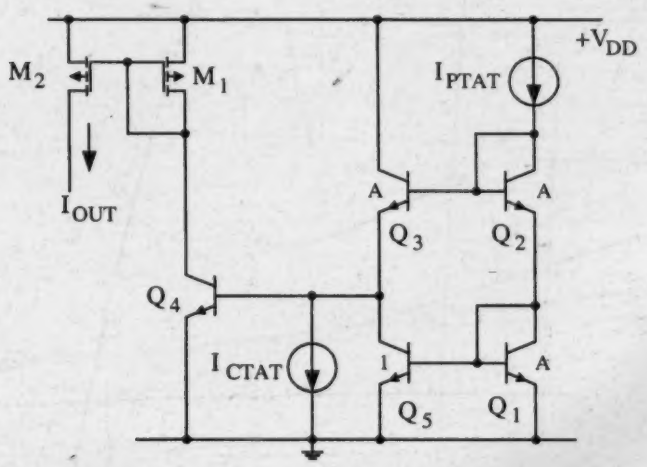

Figure 4.6 PTAT^2 current reference using a bipolar trans-linear circuit

Analog trans-linear circuits can also be used in generating PTAT^2 current. Figure 4.6 shows a PTAT^2 current reference designed with BJT transistors. Applying KVL for the loop consisting of transistors Q_1, Q_2, Q_3, and Q_4 one obtains that

$$V_{BE3} + V_{BE4} = V_{BE2} + V_{BE1} \tag{4-25}$$

Applying the result (4-3) to this equality one can then obtain

$$I_{PTAT^2} = I_{C4} = \frac{I_{C1} I_{C2}}{I_{C3}} = \frac{(I_{PTAT})^2}{(I_{PTAT}/A) + I_{CTAT}} = \frac{(I_{PTAT})^2}{K} \tag{4-26}$$

where A is the emitter area of transistors Q_1 to Q_3. The circuit is designed in such a way that $(I_{PTAT}/A) + I_{CTAT} = K$ is a constant in the desired temperature range. Then I_{C4} will indeed be proportional to the square of the temperature.

4.5 Summary

Current references are essential building blocks in analog and digital circuits. This chapter considered some basic representative circuits of current references with different temperature dependencies of the reference current.

A PTAT current reference generates a current proportional to temperature. The basic design for this type of current reference applies a PTAT voltage, easily obtained as the difference of two base-emitter voltages, across a temperature-independent resistor. This is the current source that is very frequently used in the first-order bandgap references (one may notice that this type of bias current was used in the circuits of Chapter 2).

The current generated by a CTAT current reference has a negative temperature coefficient. This current is obtained applying a single base-emitter voltage to a temperature-independent resistor. The proper combination of PTAT and CTAT currents results in a reference with temperature-independent current.

Finally, an example of a design that gives $PTAT^2$ current reference was considered. This type of current reference is the most frequently used in the design of precise curvature-compensated bandgap references, and is especially suitable for modern CMOS technologies. The detailed consideration of these references is outside of the scope of this thesis (however, some basic consideration will be given in Chapter 5). The interested reader may consult reference [1].

Chapter 5 Curvature-Compensated Bandgap Voltage References

Typical first-order bandgap references are not adequate for high-performance systems such as data and power converters [1, 2]. Therefore, higher-order references are in a great demand for such precise applications, and this has been resulted in the continuing development of many higher-order temperature compensation techniques. In 1978, Widlar proposed a bandgap reference as an attempt to provide second-order temperature compensation [46]. In his design he used different temperature behaviors for the collector currents generating the base-emitter voltages. Soon a second-order curvature compensated reference using resistor ratio proposed by Lewis and Brokaw [47].

Later on many high-order temperature compensation techniques, such as exponential temperature compensation developed by Lee *et al.* [48], piecewise-linear curvature correction presented by Rincon-Mora et al. [50], and quadratic temperature compensation proposed by Song *et al.* [4], were developed. The development of new techniques for curvature-compensated bandgap references is still continuing [50, 51, 52] at all levels of the power supply voltage.

This chapter reviews the most popular representatives of this type of reference. In the first-order references only the linear term of base-emitter voltage temperature dependence is compensated. The higher order terms are left uncompensated resulting in the characteristic parabolic curvature variation of the output voltage with temperature. The higher-order bandgap references with compensation try to compensate, in addition to the linear term, some other terms (most frequently the term proportional to the second degree of temperature) of this residual quadratic law type dependence. The dependence of the output voltage versus temperature after this compensation will have the characteristic "lazy-S" form. The higher-order references (in the sense that the expansion for emitter-base voltage dependence from temperature includes the terms higher than the linear one) are also known as curvature-corrected or curvature-compensated references.

5.1 Direct solution

Several approaches have been suggested for curvature correction. One straightforward solution, which does not consider the compensation of a particular term in the expansion of $V_{BE}(T)$ in the Taylor's series, is to design the current source I_C, with temperature dependence

$$I_C = DT^x, \tag{5-1}$$

and to use this current source as the bias current. One has to choose $x = 4 - m$ so that in the temperature dependence

$$V_{BE} = V_{g0} - \frac{T}{T_r}[V_{g0} - V_{BE}(T_r)] - [(4-m)-x]V_T \ln\left(\frac{T}{T_r}\right) \tag{5-2}$$

the last term becomes equal to zero. The exact value of m is usually not known, and one possible solution [41] is to develop the series of current generators with $x = 0.5$, 1, 1.5, 2, 2.5 .... Choosing x so that $(4-m)-x$ is the smallest value one hopes to achieve the most linearized dependence $V_{BE}(T)$ that can be compensated by the PTAT dependent voltage. This method is the most suitable for realization in BiCMOS technology that, at the present time, has practically disappeared from manufacturing.

However, the investigation [17] shows that in modern CMOS technologies m is sufficiently close to 2. Then, if one uses the current source with $x = 2$, i.e. PTAT^2 current source for biasing, the residual nonlinear term in (5-2) will be sufficiently small. This may explain the popularity of compensation methods, direct as well as indirect ones, using this type of the current source.

The basic idea behind many other curvature-compensated references is to simply add a curvature-correcting component of the bias current that increases with temperature in a nonlinear fashion. The designer hopes that, in this case, the bias current will have a sufficient PTAT^2 current component to compensate the second, and may be even higher than the second order terms.

5.2 Curvature compensation using the PTAT^2 voltage

The design of many precise bandgap references is based on the cancellation of the second-order term in the Taylor-series expansion of (5-2) that was given in Chapter 3 and is repeated here for convenience:

$$V_{BE}(T) = a_0 + a_1\frac{\Delta T}{T_r} + a_2\left(\frac{\Delta T}{T_r}\right)^2 + a_3\left(\frac{\Delta T}{T_r}\right)^3 + \ldots + a_n\left(\frac{\Delta T}{T_r}\right)^n + O\left[\left(\frac{\Delta T}{T_r}\right)^{n+1}\right] \quad (5\text{-}3)$$

Hence, one can compensate the second-order term of this temperature dependence by adding a PTAT^2 voltage to the output voltage of a first-order bandgap reference (which, in turn, includes the sum of V_{BE} and $A_{VT}V_T$ voltages). Figure 5.1 shows the concept of such curvature compensation (the components are not in scale). Since the PTAT^2 voltage is small for the lower part of the temperature range, the output waveform shows the curvature of a first-order bandgap reference. However, as the temperature increases the PTAT^2 term becomes increasingly large and cancels the increasing negative component in the temperature dependence of the base-emitter voltage. Consequently, one obtains a nearly constant reference voltage V_{REF} that includes the temperature-dependent component with the characteristic curvature shown in this figure.

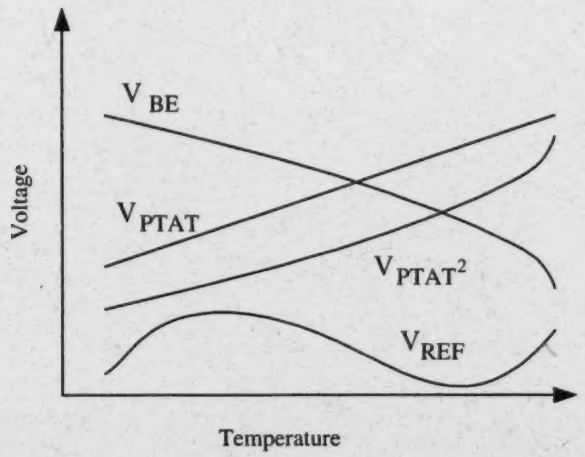

Figure 5.1 Curvature-compensation concept using a PTAT^2 voltage

One implementation of this voltage compensation technique with indirect approach is illustrated in Figure 5.2 [4].

All three currents I_0 shown in this figure are temperature-independent and the PTAT current I_T is given by

$$I_T = \alpha V_T + \beta \tag{5-4}$$

where α and β are constants. The output voltage V_{REF}, can be expressed as

$$V_{REF} = V_{EB} + G(V_{EB2} - V_{EB1}) = V_{EB3} + G\Delta V_{EB} \tag{5-5}$$

where

$$\Delta V_{EB} = V_T \ln\left(A\frac{I_0 + I_T}{I_0 - I_T} \right) \tag{5-6}$$

and A is the emitter area ratio of Q_1 and Q_2, and G is the amplifier gain. The Taylor series expansion of (5-6) will result in

$$\Delta V_{EB} = V_T \ln A + 2V_T\left(\frac{I_T}{I_0}\right) + \frac{2}{3}V_T\left(\frac{I_T}{I_0}\right)^3 + \ldots \tag{5-7}$$

Substituting (5-7) into (5-5), and neglecting higher order terms one obtains

$$V_{REF} \approx V_{EB3} + GV_T \ln A + G\frac{2\alpha}{I_0}V_T{}^2 \tag{5-8}$$

As one can see, a PTAT^2 voltage appears in the output voltage. The transistor Q_3 is biased by a temperature-independent current ($x = 0$), so $V_{EB3}(T)$ should include, in addition to the linear term, a PTAT^2 term as well. The linear term will be compensated by the $GV_T \ln A$ term, and the PTAT^2 term will be compensated by the $G(2\alpha / I_0)V_T{}^2$ term if the design parameters are properly chosen (they can be found by simulations). The experimental results show average temperature coefficients of 13 and 26 ppm/°C over the commercial and military temperature ranges, respectively.

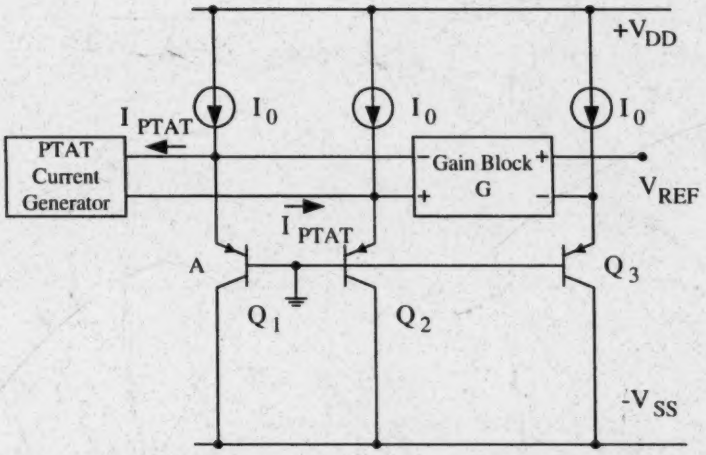

Figure 5.2 Curvature-compensated BGR using a PTAT^2 voltage component

5.3 Curvature Compensation Using the Temperature-Dependent Resistor Ratio

Another technique for canceling high-order components of $V_{BE}(T)$ is to generate a nonlinear component by exploiting the temperature dependence of different resistive materials.

Figure 5.3 shows a circuit based on this techniques [50]. In this circuit resistors R_1, R_2 and R_4 are implemented by using the same material, and resistor R_3 is implemented by a different material. The PTAT current I, generated by transistors Q_1 and Q_2 and resistor R_1 is given by

$$I = \frac{V_T \ln N}{R_1} \tag{5-9}$$

as usual. In (5-9) N is the emitter area ratio of Q_1 and Q_2. This current is passed through resistors R_2 and R_3, and so the output voltage V_{REF} is expressed as

$$V_{REF} = V_{EB2} + \left(\frac{R_2}{R_1}\ln N\right)V_T + \left(\frac{R_3}{R_1}\ln N\right)V_T \tag{5-10}$$

The resistor ratio R_2/R_1 is temperature-independent since both resistors are implemented using the same material. However, the ratio R_3/R_1 is temperature-dependent due to the material difference, and so the third term in (5-10) generates the desired nonlinear component which leads to curvature compensation of the output voltage.

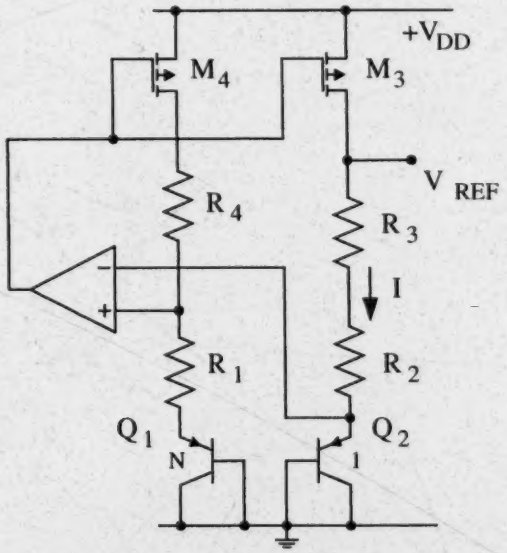

Figure 5.3 Curvature-compensated BGR using temperature dependency of resistor ratio

For temperature trimming, an optimum R_3/R_1 should be found such that the nonlinear error voltage is minimized. Then, the linear temperature dependence of the output voltage should be minimized by finding an optimum R_2/R_1. Experimental measurements show an average temperature drift of 5.3 ppm/°C over the temperature range 0-100 °C.

The advantages of this technique over using PTAT^2 approach are simplicity and cost effectiveness. Only one additional resistor is required to convert a first-order bandgap reference into a second-order compensated circuit. However, there is one significant disadvantage: the performance of this circuit is highly dependent on the process and

the temperature of the resistor ratio, R_3 / R_1, which varies substantially from process to process [1].

5.4 Curvature Compensation Using Nonlinear Currents

A nonlinear current can also be used for generating the curvature-correcting component. This nonlinear current can be exponential [48] or piecewise linear [49]. Figure 5.4 shows a circuit used for generating a piecewise-linear current [49]. Transistor M_2 is biased with $K_1 I_{PTAT}$ current. For the lower part of the temperatures, when $K_2 I_{VBE} > K_1 I_{PTAT}$ and transistor M_2 is forced to operate in the triode region ($I_{M1} = K_1 I_{PTAT}$), consequently, M_3 does not

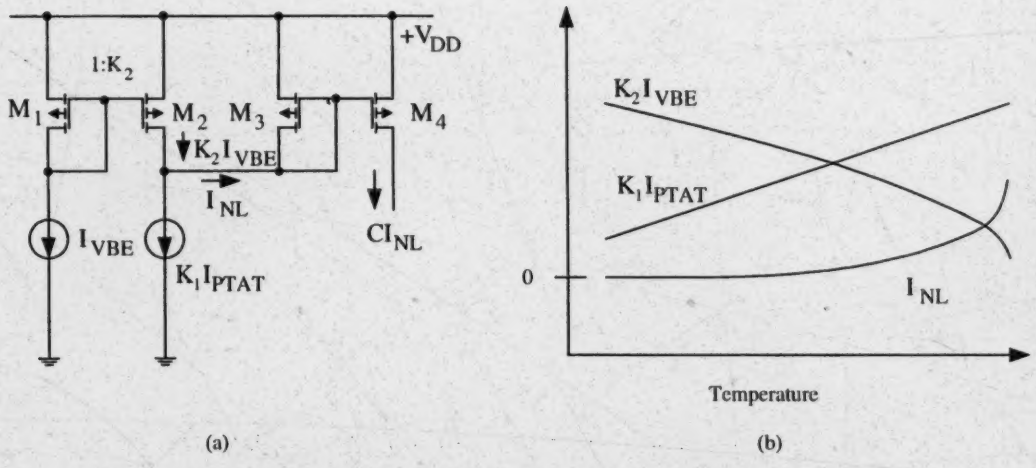

Figure 5.4 Generation of the nonlinear current (a) circuit (b) currents

conduct any current and I_{NL} is equal to zero. For the upper part of the temperature range, $K_1 I_{PTAT}$ becomes larger than $K_2 I_{VBE}$. Therefore, M_2 enters saturation and sup-

plies $I_{M1} = K_2 I_{VBE}$, forcing M_3 to source the difference of $K_2 I_{VBE}$ and $K_1 I_{PTAT}$. The resulting current I_{NL} is nonlinear and can be described by

$$I_{NL} = \begin{cases} 0 & (I_{VBE} \geq I_{PTAT}) \\ K_1 I_{PTAT} - K_2 I_{VBE} & (I_{VBE} < I_{PTAT}) \end{cases} \tag{5-11}$$

where K_1 and K_2 are constants defined by the ratios of the mirroring transistors defining I_{PTAT} and I_{VBE}.

Curvature correction then can be obtained by combining the three temperature-dependent currents I_{VBE}, I_{PTAT} and I_{NL} (Figure 5.5).

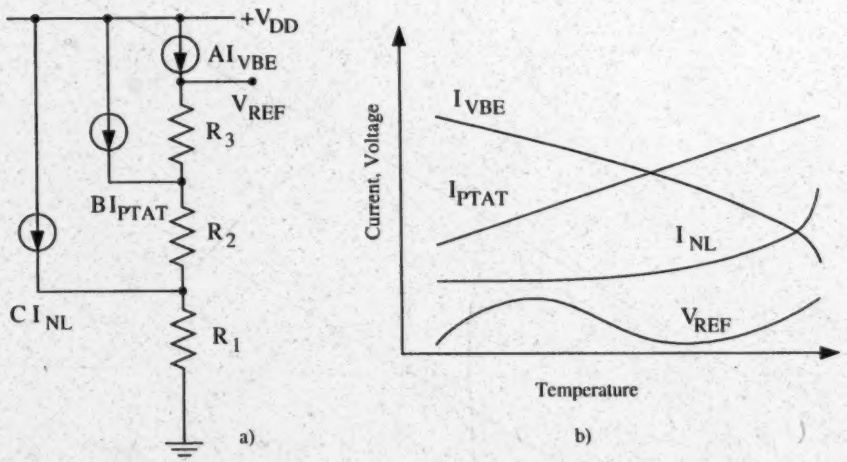

Figure 5.5 Piecewise linear curvature-corrected voltage reference

The output voltage in this reference is given by

$$V_{REF} = AI_{VBE}(R_1 + R_2 + R_3) + BI_{PTAT}(R_1 + R_2) + CI_{NL}R_3 \tag{5-12}$$

A typical behavior of output voltage for this circuit is shown in Figure 5.5(b). For the lower part of temperature range, the current I_{NL} is very small (it is close to zero), and the circuit behaves like a first-order bandgap reference. For the upper part of the temperature range, the combination of these three currents diminishes the nonlinear effect

of the base-emitter voltage. Experimental measurements [49] show an average temperature drift of 20 ppm/°C over the temperature range from –15 to 90°C.

5.5 Summary

Typical first-order bandgap references are not adequate for high-performance systems such as data and power converters. Therefore, higher-order references are in a great demand for such precise applications, and this has resulted in the development of many high-order temperature compensation techniques. The development of these techniques now is the main stream of bandgap reference design. This chapter reviewed the most popular representatives of this type of references. In the first-order references only the linear term of base-emitter voltage temperature dependence is compensated. The higher order terms are left uncompensated resulting in the characteristic parabolic curvature variation of the output voltage across temperature. The bandgap references with compensation try to compensate, in addition to the linear term, some terms (most frequently only one) of this residual quadratic law type dependence of the output voltage versus temperature. This is the reason why the higher-order references (in the sense that the expansion for emitter-base voltage dependence from temperature includes the terms higher than the linear one) are also known as curvature-corrected references.

The basic idea behind of many other curvature-compensated references is to simply add a curvature-correcting component of the bias current that increases with temperature in a nonlinear fashion. The designer hopes that in this case this bias current will help to compensate higher than the second order terms. Simulations are used to establish the best result. The curvature compensation does not remove the problem of operation with a low voltage power supply. Moreover, many techniques require an increase of the power supply voltage.

Chapter 6 Non-Bandgap Voltage References Using the ZTC Point

In the previous chapters we studied the theory and techniques used for the design of bandgap voltage references. It was shown that the output voltage of a bandgap reference has a high power supply rejection ratio (PSRR) and a very small temperature coefficient, and is stable against process variations. However, IC design is now dominated by low power, low voltage objectives making CMOS the technology of choice. The bandgap voltage reference is bipolar in nature. It is, after all, using a p-n junction voltage drop V_{BE}. The circuits of this type, no matter how the compensation of V_{BE} temperature dependence is achieved, must have the power supply voltage higher than 0.7 V. The best result, as we know, is achieved by direct compensation, when the generator of compensation voltage with positive temperature coefficient is connected in series with V_{BE} voltage. This approach is realized when the power supply voltage is above 1.25 V (about 1.5 V in practical circuits). As soon as the supply voltage is below 1 V, and only indirect compensation methods (for example, using voltage to current transformation) can be used, the bandgap references do not show good stability [36, 37]. Therefore, IC designers are challenged with designing circuits that can be implemented in low cost CMOS technology and their performances are comparable to the performance of the bandgap voltage references.

In this chapter, we review non-bandgap references that use the ZTC point. They were developed in this department over the last several years [17, 53, 54]. The issues, with respect to temperature, that surround the design of these references were studied in Chapter 2.

6.1 Voltage regulator type reference using compensation of threshold voltage and mobility temperature effects

The first sub-1V power supply voltage reference using compensation of threshold voltage and mobility temperature effects, and compatible with standard CMOS technologies is shown in Figure 6.1. The circuit is designed using the voltage regulator approach [55], and is similar to the references with Zener diode and operational amplifiers. It was designed under the assumptions (see Chapter 2) that $\alpha_{\mu 0} = -2$, $\alpha_{VT} = -0.83$ mV/°C, I_{DF} =192 μA and V_{GSF} =869 mV.

The reference includes a standard two-stage operational amplifier. The input stage consists of the differential pair Q_2, Q_3 with active loads Q_4, Q_5. The output stage is the common source transistor Q_9 with active load Q_8. The output of this amplifier biases Q_1 in the point of zero temperature coefficient (ZTC point) characterized by the gate-source voltage V_{GSF} and the current I_{DF}. Hence, the voltage $V_{OUT} = V_{GSF}$ is temperature-independent and may be used as a reference voltage. To provide the required voltage at the branch including R_3 and Q_3 the reference includes the second feedback loop via divider R_1 and R_2. The resistors should be chosen so that the current through R_3 will be equal to

$$I_{D1} = I_{DF} = V_{GS1}\frac{R_2}{R_1 R_3} = V_{GSF}\frac{R_2}{R_1 R_3} \qquad (6\text{-}1)$$

The reference was realized in 0.35-μ m CMOS technology [17]. The values of I_{DF} =192 μA and V_{GSF} =869 mV were obtained in preliminary simulations for the n-channel device with W/L=50μm/2.5μm, and were considered as the parameters of the ZTC bias point at $T = T_0$=300°K.

The Figure 6.1 aspect ratios are given in micron/micron. The technology parameters used for the calculations were $\mu_n C_{ox}$ = 210 μA/V² and $\mu_p C_{ox}$ = 70 μA/V², V_{TN} =0.6 V, V_{TP} = –0.7 V. The operational amplifier is compensated by a capacitor C_C = 10 pF. The amplifier transconductance, G_T, is equal to 142 mA/V when the circuit is biased

by the external bias current I_{BIAS}=44μA applied to the terminal IBIAS. The transistor Q_1 in this case should have I_{D1}=193μA and V_{GS1}=870 mV, the values close to the required ones. The resistors are $R_1 = 10$ kΩ, $R_2 = 5.8$ kΩ, and $R_3 = 2.6$ kΩ.

When we change the temperature, the resistor values also change so that $R_i = R_{i0}(1 + k_i \Delta T)$ (here $i = 1,2,3$). Substituting these dependencies into (6-1) one finds that the variation ΔI_D, of the I_{DF} current due to the resistor temperature variations is given by the equation

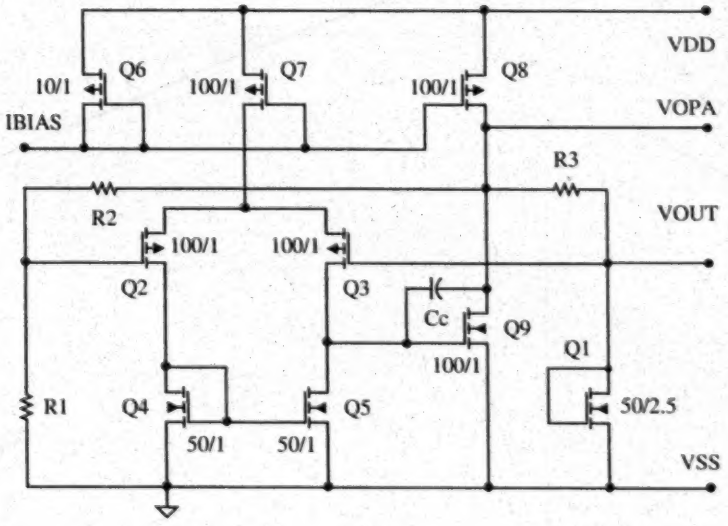

Figure 6.1 Voltage reference of regulator type

$$I_{DF} + \Delta I_D \approx V_{GSF} \frac{R_{20}}{R_{10} R_{30}} [1 + (k_2 - k_1 - k_3)\Delta T] \qquad (6\text{-}2)$$

This result shows that $\Delta I_D \approx 0$ when

$$k_2 = k_1 + k_3 \qquad (6\text{-}3)$$

This condition for temperature coefficients is satisfied rather closely in 0.35-μm CMOS technology if R_1 and R_3 are implemented using the polysilicon resistor layer ($k_1 = k_3 = 0.722*10^{-3}$ 1/°C), and R_2 is implemented using the n^+-diffusion layer ($k_2 = 1.473*10^{-3}$ 1/°C).

It was shown [17] that, in case of $\alpha_{\mu 0} \neq -2$, this reference may be tuned by an external bias current I_{BIAS}, so that the output voltage temperature dependence is described by the formula

$$V_{OUT} = V_{REF} + A_2\left(\frac{\Delta T}{T_0}\right)^2 \tag{6-4}$$

where

$$V_{REF} = V_{GSF} + (2+\alpha_{\mu 0})\left((\alpha_{VT}T_0/\alpha_{\mu 0}) + V_{GSF}\right) \tag{6-5}$$

and

$$A_2 = -\left[(2+\alpha_{\mu 0})\frac{\alpha_{VT}T_0}{\alpha_{\mu 0}} + \alpha_{\mu 1}\left(\frac{\alpha_{VT}T_0}{\alpha_{\mu 0}} + V_{GSF}\right)\right] \tag{6-6}$$

In (6-6), the $\alpha_{\mu 1}$ is the temperature coefficient in the temperature dependence of the parameter

$$\alpha_\mu = \alpha_{\mu 0} + \alpha_{\mu 1}\left(\frac{\Delta T}{T_0}\right) \tag{6-7}$$

This reference circuit was fabricated, and Figure 6.2 gives the test results. Changing the bias current by an external temperature-stable resistor, each sample was tuned to the same output voltage $V_{OUT} = V_{REF} = 799$ mV. Then, indeed, the output voltage temperature dependence was seen to be approximated by a quadratic law as given by (6-4). The average temperature stability of these references was about 10 ppm/°C over the temperature range of -20 °C to 100 °C. The stability was in the worst case 15 ppm/°C for the same temperature range.

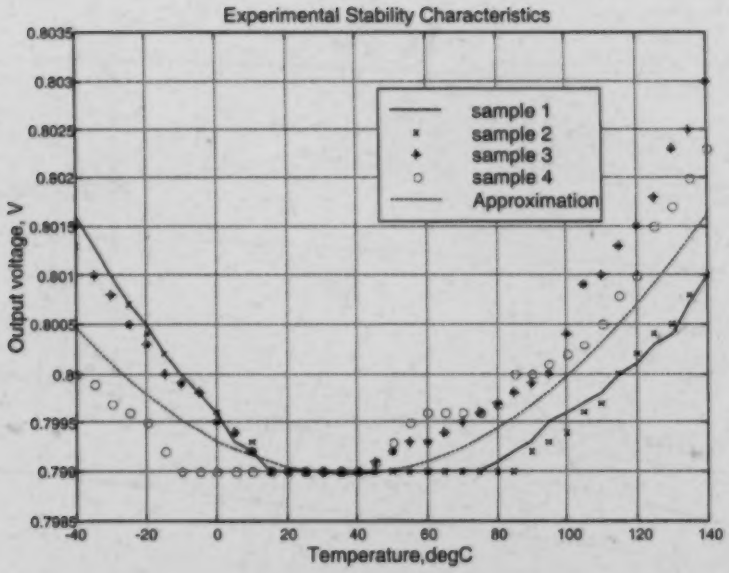

Figure 6.2 Experimental temperature stability characteristics

There are two important restrictions in the design of this circuit. The first one is given by (6-3). This relationship does not exist, for example, in the smaller scale 0.18-μm technology that followed the 0.35-μm technology. In addition, the ZTC point, located at nearly 0.8 V, requires that the reference be designed for a power supply voltage at least about 1 V.

Fortunately, the ZTC point in 0.18-μm technology has moved down to 0.72 V. This fact, together with high temperature stability of the previously designed reference, stimulated a search for references that use compensation of threshold voltage and mobility temperature effects, ones that do not require any special relationship between the thermal coefficient of resistors and, in the worst case, require only matched and tracking resistors.

6.2 Compensation reference using PTAT bias sources and voltage balance

When the transconductance characteristics have a ZTC point, the voltage reference for low-voltage power supply may be also realized in a standard CMOS technology, using PTAT current sources. These current sources are used to bias two diode-connected NMOS transistors, both operating below the ZTC point, so that the drain voltages of these transistors will have opposite temperature coefficients (Figure 6.3). Then, on the resistor connecting these two drains, one can find a point where the voltage does not change with temperature.

Figure 6.3 shows the simulated current-voltage characteristics (with temperature as a parameter) for a normal NMOS transistor in 0.18μm CMOS technology. The ZTC point is clearly shown in the figure. Assume that this transistor is diode connected and biased with the PTAT current $I_D(T)$, which can be expressed as

$$I_D = I_{D0}(1+\gamma(T-T_0)) \tag{6-8}$$

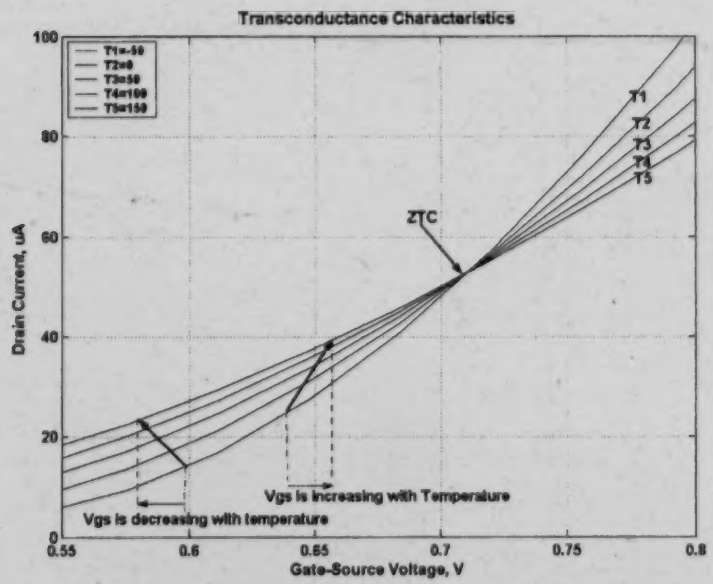

Figure 6.3 Transconductance characteristics of the NMOS transistor

where T_0 is the reference temperature and γ is a positive constant. Following [17], [56] and [10], the gate-source voltage of an NMOS transistor can be written as

$$V_{GS}(T) = V_{TH0} + \alpha_{VT}(T - T_0) + K(\frac{T}{T_0})^{\frac{m}{2}}\sqrt{I_D(T)} \tag{6-9}$$

where T_0 is the reference temperature, m is positive constant and α_{VT} is negative constant, and $K = \sqrt{\frac{2}{\mu_0 C_{ox}(W/L)}}$. In (6-9) we have assumed that the threshold voltage V_{TH}, decreases with temperature linearly as $V_{TH} = V_{TH0} + \alpha_{VT}(T - T_0)$, and the mobility $\mu(T)$, depends on temperature as $\mu(T) = \mu_0(\frac{T}{T_0})^{-m}$. At $T = T_0$ the gate-source voltage is equal to

$$V_{GS}(T_0) = V_{TH0} + K\sqrt{I_{D0}} \tag{6-10}$$

Now, if the temperature is increased by a small amount, δT, the gate-source voltage of the above transistor will be equal to

$$V_{GS}(T_0 + \delta T) = V_{TH0} + \alpha_{VT}\delta T + K(1 + \frac{\delta T}{T_0})^{\frac{m}{2}}\sqrt{I_{D0}(1 + \gamma\delta T)} \tag{6-11}$$

Subtracting (6-10) from (6-11), we find the change of the gate-source voltage with temperature to be

$$\delta V_{GS} = V_{GS}(T_0 + \delta T) - V_{GS}(T_0) = \alpha_{VT}\delta T + \lambda[(\sqrt{1 + \gamma\delta T})(1 + \frac{\delta T}{T_0})^{\frac{m}{2}} - 1] \tag{6-12}$$

where $\lambda = K\sqrt{I_{D0}}$. Using the approximations $\sqrt{1 + \gamma\delta T} \approx 1 + \frac{\gamma\delta T}{2}$ and $(1 + \frac{\delta T}{T_0})^{\frac{m}{2}} \approx 1 + \frac{m}{2}\frac{\delta T}{T_0}$ in (6-12), one obtains

$$\frac{\delta V_{GS}}{\delta T}|_{T=T_0} \cong (\alpha_{VT} + \frac{\lambda}{2}(\frac{m}{T_0} + \gamma)) \tag{6-13}$$

Equation (6-13) shows that, depending on the values of λ and γ, which are the PTAT current source parameters, the temperature coefficient of the gate-source voltage can be positive, negative or zero. The first two cases are clearly shown in Figure 6.3.

The proposed voltage reference circuit is shown in Figure 6.4. The circuit consists of three parts: (i) a start-up circuit (transistors M_{S1}-M_{S3}) (ii) a low-voltage standard bias circuit (transistors M_1-M_4 and resistor R_B) for the realization of PTAT currents, and (iii) the reference core circuit (two diode–connected transistors M_7 and M_8 operating below the ZTC point, and two balancing resistors R_1 and R_2). Transistors M_5 and M_6 supply PTAT currents to transistors M_7 and M_8. The loop current I_B, in the bias loop is equal to [26] (see also Chapter 4, part 4.1.2, the discussion of this part is partially repeated here for convenience)

$$I_B = A/(R_B^2 \mu(T)) \tag{6-14}$$

where $A = (2/C_{ox})\left(\sqrt{(W/L)_4} - \sqrt{(W/L)_3}\right)^2$. We assume that R_B depends on temperature as

$$R_B = R_{B0}[1+\alpha_{R1}(T-T_0)+\alpha_{R2}(T-T_0)^2] \tag{6-15}$$

Using a first-order approximation (i.e. assuming $\alpha_{R2} = 0$), one can find that the loop current I_B, in the bias circuit is equal to

$$I_B \approx I_{B0}[1+\gamma\ (T-T_0)] \tag{6-16}$$

where

$$I_{B0} = (2/C_{ox})\mu_0^{-1} R_{B0}^{-2} (\sqrt{(L/W)_4} - \sqrt{(L/W)_3})^2 \tag{6-17}$$

and

$$\gamma = \left(\frac{m}{T_0} - 2\alpha_{R1}\right) \tag{6-18}$$

Hence, a PTAT bias current is obtained using a low voltage standard bias circuit. Therefore, the drain currents of M_5 and M_6, as well as the drain currents of M_7 and M_8, will be also increasing with temperature, with the same γ as the reference current I_B.

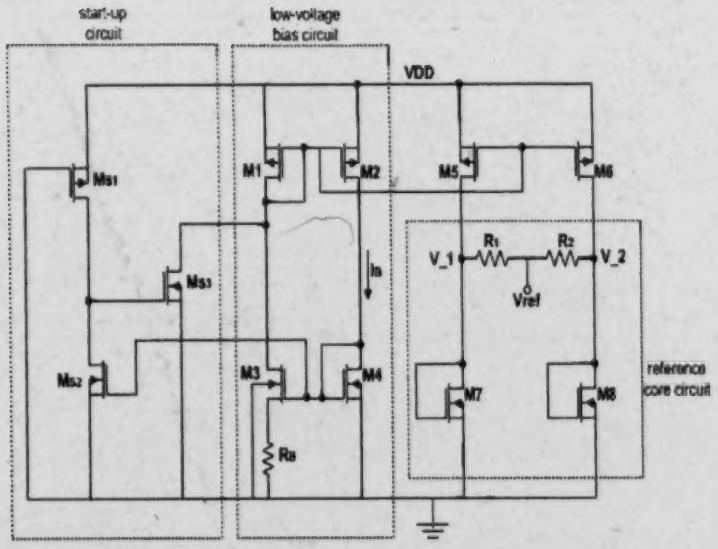

Figure 6.4 The voltage reference with balancing resistors

The diode-connected transistors M_7 and M_8 have the same length and width to ensure that their threshold voltage characteristics are sufficiently close. Then the output voltage is given by

$$V_{ref} = \frac{V_1}{1+\frac{R_1}{R_2}} + \frac{V_2}{1+\frac{R_2}{R_1}} \tag{6-19}$$

Assume that $R_1 = R_2$, and they are matched resistors with good tracking ability. Using (6-19) and (6-13) for transistors M_7 and M_8, one can find that the change of the voltage reference output δV_{ref}, with respect to the temperature, will be equal to

$$\delta V_{ref} = 0.5(\delta V_{GS7} + \delta V_{GS8}) = \delta T[2\alpha_{VT} + (\lambda_7 + \lambda_8)(\frac{m}{2T_0} + \frac{\gamma}{2})] \tag{6-20}$$

To have a temperature-insensitive output voltage, λ_7 and λ_8 (or, in fact, the sizes of transistors M_5 and M_6) should be chosen to satisfy

$$2\alpha_{VT} + (\lambda_7 + \lambda_8)(\frac{m}{2T_0} + \frac{\gamma}{2}) = 0 \qquad (6\text{-}21)$$

This will happen when the temperature coefficient of the gate-source voltage for one of the transistors (M_7 or M_8) is positive and for the other one is negative.

The output voltage depends on the ratio of the resistors R_1 and R_2, thus the sensitivity of the output voltage to variation of the resistors (due to non-optimized layout) is reduced.

Since the threshold voltage is maximally at the lowest operation temperature, the minimum supply voltage should be considered at this temperature. The minimum supply voltage for the this voltage reference is given by

$$V_{DD\min} = (V_{THN})_{\max} + |V_{DS5}(sat)| \qquad (6\text{-}22)$$

Therefore, it is possible for the proposed voltage reference to operate with a sub-1 V supply.

The circuit shown in Figure 6.4 was designed for realization in 0.18-μm TSMC technology. All the resistors are realized using N+ without silicide diffusion layer and their temperature dependencies are given by (6-15) and $\alpha_{R1} = 1.47 \cdot 10^{-3}$ deg^{-1}and $\alpha_{R2} = 0.832 \cdot 10^{-6}$ deg^{-2} for all resistors. The circuit was simulated over the temperature range of -50^{o}C to 150^{o}C. Figure 6.5 shows the simulation results for the currents I_B , I_7 and I_8 . The simulation results for gate-source voltage of transistors $M_7$and M_8 and the output voltage V_{ref} are shown in Figure 6.4. The temperature stability of the voltage reference output V_{ref} (see Table 6.1) obtained in

Table 6.1 Temperature stability of different voltage references

Technique	Temperature stability (ppm/ ^{o}C)
Bandgap reference [36]	59
CMOS Voltage-Reference based on V_{TH} difference [57]	33.8
CMOS Voltage Reference proposed in [58]	36.9
CMOS Voltage Reference using ZTC point [17]	13
This Voltage Reference	4

simulations is equal to 4 ppm/ ^{o}C .

Since the temperature-dependence of the threshold voltage and the reference current are not exactly linear in the whole temperature range, there is a nonlinear residue appearing on the reference voltage output.

The reference was fabricated and tested. The experimental temperature stability was as in simulations but for a more narrow temperature range of -20 to 90 ^{o}C [59]. The reasons for the difference between simulated and experimental results at the edges of the temperature range were never investigated.

Table 6.1 also compares the temperature performance of the proposed voltage reference with previously designed references. This table is arranged the following way. The first line shows the result for the sub 1-V bandgap reference. All other lines show the results for nonbandgap references which may be potentially designed for the sub 1-V power supplies. These results were very encouraging. They show that, instead of complicated compensated bandgap reverences where the power supply cannot be reduced below 0.9 V anyway, one may try to design nonbandgap references with more

potential for reduction in the power supply voltage. The references investigated in the following chapter confirmed this point of view.

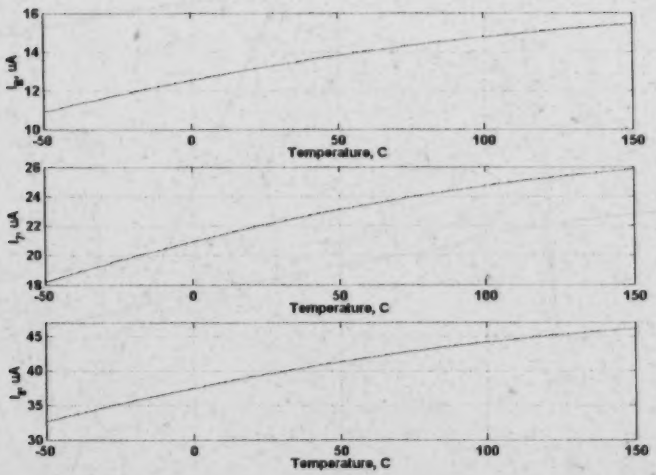

Figure 6.5 Temperature dependencies of the currents I_B, I_7 and I_8

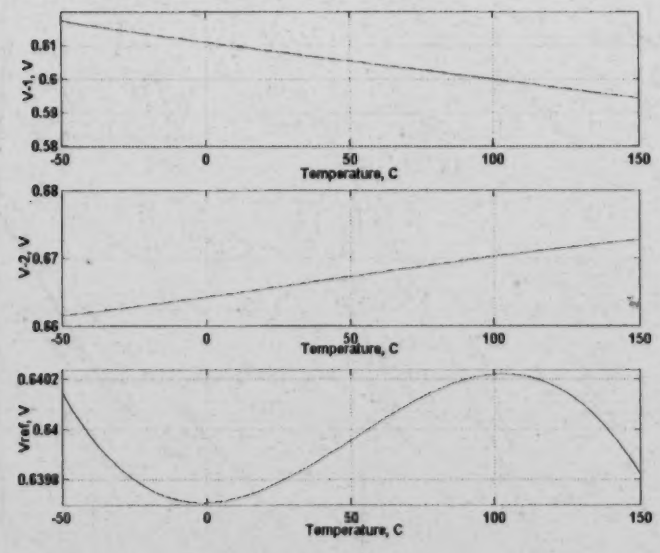

Figure 6.6 Temperature dependencies of the voltages V_1, V_2 and V_{ref}

6.3 Summary

The bandgap voltage reference is bipolar in nature. It includes a p-n junction, with a voltage drop V_{BE}. The circuits of this type, no matter how the compensation of V_{BE} temperature dependence is achieved, should have a power supply voltage higher than 0.7 V. As soon as the supply voltage is below 1 V, and only indirect compensation methods (for example, using voltage to current transformation) can be used, the bandgap references do not show good temperature stability. Therefore, IC designers are challenged with designing circuits that can be implemented in low cost CMOS technology with performances that are comparable to the performance of the bandgap voltage references.

In this chapter we discussed non-bandgap references using ZTC point. Their development presented in this chapter was not focused on design for low power supply voltage (even though some of them allow operation with the supply voltage below 1V). The main purpose of this demonstration was to show that it is possible to design the references of nonbandgap type having high temperature stability of the output voltage. Moreover, in the conditions of not very low supply voltages, they allow further improvements that can be used in design of bandgap references.

Chapter 7 Voltage References Based on Threshold-Voltage-Difference Architecture

The main step to realize a voltage reference is to find a stable physical voltage, such as the bandgap voltage used in bandgap voltage references. But the bandgap voltage of silicon is about 1.215 V. This means that the references with the output voltage equal to the bandgap voltage should definitely have a power supply voltage higher than 1.215 V, and the usual figure is about 1.5 V [33]. The emitter-base voltage that is related to the bandgap voltage is about 0.7 V, and the references based on the base-emitter voltage temperature compensation should have power supply higher than 0.7 V. The most successful designs operate from the power supply of 0.84 V [36]. To design the reference that is able to work with a power supply less than 0.7 V one has to find the voltages that are less than 0.7 volts, and at the same time, stable with temperature.

Such a voltage, for example, can be created using the MOS transistor threshold voltage (which is usually less than 0.5 V in absolute value for modern CMOS technologies) and then compensating its temperature dependence (which is linear) by another threshold voltage. The first attempt to build a nonbandgap reference based on this principle can be found in [7]. The NMOS technology reference described in this work uses compensation of the temperature dependence of an enhancement transistor by the temperature dependence of a depletion transistor. This technology does not exist anymore, yet it achieved in [7] a temperature coefficient of 6ppm/^{o}C. This shows that using transistors with different thresholds and the same type of carriers in channels, one can obtain a temperature stable voltage, and the temperature coefficient of this voltage may be comparable with that of bandgap references. This fact is a crucial one for the design approach of this chapter, even though the circuits investigated here are different from that of [7].

If the transistors have channels of different carrier nature (i.e. one is p-channel, the

other is n-channel), and the thresholds have different absolute values, the difference of the thresholds is also relatively temperature-stable [45]. This difference was used to design a nonbandgap reference in one of the older CMOS technologies [58], with a reference voltage temperature coefficient of about 37 ppm/°C. Yet, the design of the reference [58] requires satisfying two design conditions. One is concerned with the relationship between resistors and the temperature coefficients of threshold voltages; another, more complicated, involves transistor sizes, the exponents of p- and n-mobility temperature dependencies, and the temperature coefficients of threshold voltages. These two conditions make the design of references considered in [58] impractical. We therefore tried to find a different approach suitable for modern CMOS technologies.

In modern CMOS multi-threshold technologies, all transistors are of the enhancement type. Three possible solutions for the standard 0.18-μm CMOS technology are proposed in this chapter. All references are based on the difference of the absolute values of threshold voltages existing for the devices (altogether five types of devices are available) in modern versions of this technology.

The first type of reference is an original design. In this circuit the voltage $|V_{T1}|-|V_{T2}|$ is applied to a resistor. Then a current mirror is used to transfer this current to the output resistor. The voltage developed at the output resistor is proportional to the difference $|V_{T1}|-|V_{T2}|$ of two threshold voltages. Different reference voltages are obtained by substituting different transistors in the same basic circuit. In the design of the basic circuit we also used the assumption that the mobility of p- and n-channel transistors track each other and that the ratio μ_n/μ_p is nearly constant with temperature as well. The results of simulations provided in this chapter investigate the validity of these assumptions.

The second type of reference is similar to the one proposed in [60]. However, the reference [60] is realized in expensive SOI technology, and requires that, similar to [7], transistors with channel depletion are also available. In CMOS technology the reference similar to this type, and investigated in this chapter (we call it, after [7],

Blauschild's voltage reference), can be realized using enhancement transistors only. One of these transistors is of regular type, with V_{TN} = 0.47 V, another is the medium threshold transistor with $|V_{TP}|$ = 0.17 V. The current mirror establishes two equal currents in these transistors of different thresholds, and an operational amplifier keeps this condition. One can set the design requirements in such a way that the operational amplifier output voltage will be equal to the difference of the threshold voltage values.

Finally, the third reference is also an original design. It uses an asymmetric differential pair loaded by an asymmetric active load. This one-stage amplifier has 100% feedback around it. The output voltage of this amplifier is equal to the difference of the gate-source voltages of two transistors with different thresholds. If the tail current of this amplifier is constant, then the output voltage of the amplifier has weak temperature dependence and can be used as a reference voltage.

7.1 Voltage references with resistor

7.1.1 Voltage reference circuit

The basic circuit for the proposed references [61] is shown in Figure 7.1. It includes an operational amplifier that keeps equal the voltages at the branches with transistors M_1 and M_2. These transistors should have different absolute values of the threshold voltages. One can use the transistors of the same polarity as well as of the opposite polarities (all possible combinations are listed below). The circuit also includes a current mirror M_3, M_4 that keeps the currents in the devices M_1, M_2 equal, and the current in the output device M_5 is equal to KI_1. The output voltage is taken at the resistor (or resistor combination, see below) connected to the drain of the output device.

If the operation of each device is described by the quadratic law [9], and the currents in M_1, M_2 are equal, then

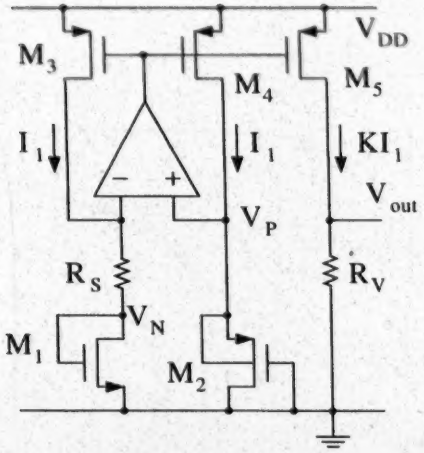

Figure 7.1 Basic voltage reference circuit

$$V_N = V_{TN} + \sqrt{\frac{2I_1}{(\mu C_{ox})_n (W/L)_1}} \tag{7-1}$$

and

$$V_P = |V_{TP}| + \sqrt{\frac{2I_1}{(\mu C_{ox})_p (W/L)_2}} \tag{7-2}$$

The difference is thus

$$V_P - V_N = |V_{TP}| - V_{TN} + \sqrt{2I_1}\left(\frac{1}{\sqrt{(C_{ox}\mu)_p (W/L)_2}} - \frac{1}{\sqrt{(C_{ox}\mu)_n (W/L)_1}}\right) \tag{7-3}$$

Let the device sizes are chosen so that

$$\frac{(W/L)_2}{(W/L)_1} = \frac{(\mu C_{ox})_n}{(\mu C_{ox})_p} \approx 2-3 \tag{7-4}$$

If this ratio is constant (i.e. the mobility track one another with temperature) then

$$V_P - V_N = |V_{TP}| - V_{TN} \tag{7-5}$$

and, as it was mentioned before, this difference is nearly constant with temperature. The quadratic law of the drain current versus gate-source voltage used in derivation (7-1)-(7-5) may be used for a limited range of currents for the devices in submicron technologies. One has to obtain this range for M_1, M_2 by preliminary simulations.

If $(W/L)_5 = K(W/L)_4$ the reference output voltage becomes

$$V_{out} = K(R_V / R_S)(|V_{TP}| - V_{TN}) \qquad (7\text{-}6)$$

Hence, if the resistors R_V and R_S are also tracking each other with temperature, the output voltage will be stable with temperature as well.

Notice that the output voltage does not depend on the power supply voltage. This is, of course, is valid when the operational amplifier is an ideal one.

7.1.2 Transistor realization of the reference circuits

The results given below show that output voltage stabilization is indeed achieved over the range of temperatures –25 to 125 ^{o}C, and when the power supply voltage drops from 1.8 V down to 0.6 V (in some cases one can drop the power supply voltage down to 0.5 V; the circuit is still operational). The operational amplifier is realized in all these references using the differential pair with an active load.

The circuit shown in Figure 7.2 is an example of transistor realization for the voltage reference shown in Figure 7.1. The operational amplifier includes the transistors M_7, M_8 and M_9, and M_{10}. Resistor R_S may be split into two resistors R_{S1} and R_{S2}. In general case these resistors may have different temperature coefficients. The split point of this resistor is used to bias the gate of cascoding transistor M_6 of the reference output stage. The resistor R_V may be realized as parallel connection of the resistors R_{V1} and R_{V2}. These resistors may also have different

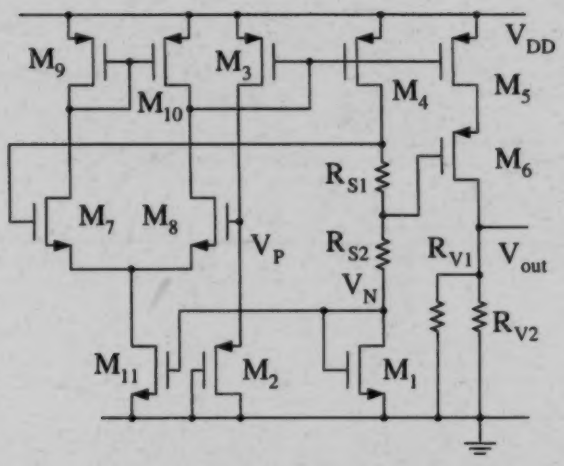

Figure 7.2 Voltage reference transistor realizations

temperature coefficients. The temperature dependence of resistors was used to compensate for insufficient tracking of μ_p and μ_n, and, hence, to improve the temperature stability of the output voltage.

In the present day CMOS 0.18-μm technology, the following transistors may be used in the circuit design. The designer may choose n-channel transistors with the threshold voltages of 0.03 V (the so-called "native, or natural, transistors" which in the Table 7.1 we denote as nan-transistors), 0.27 V (denoted here as men-transistors) and 0.47 V (denoted here as ren-transistors). The nomenclature of p-channel transistors includes the transistors with the threshold voltage of –0.17 V (denoted here as mep-transistors) and –0.46 V (denoted as rep-transistors).

Altogether we designed and simulated nine voltage references. They are listed in Table 7.1. We also show the bottom limit of the power supply voltage where the circuit is still operable.

Table 7.1 Resistor voltage references using threshold difference

Reference name	M_1	M_2	V_{DD} range
nanrep	nan	rep	1.8 V-0.8 V
nanren	nan	ren	1.8 V-1.0 V
nanmep	nan	mep	1.8 V-0.5 V
nanmen	nan	men	1.8 V-0.6 V
meprep	mep	rep	1.8 V-0.6 V
mepren	mep	ren	1.8 V-0.8 V
menrep	men	rep	1.8 V-0.8 V
menren	men	ren	1.8 V-0.9 V

All listed circuits were designed using the drain current of M_1 equal to $I_1 \approx 15\ \mu$A. The transistors M_3 to M_6 and M_9, M_{10} were mep-transistors. The transistors M_7, M_8 and M_{11} were nan-transistors.

One can see that two references allow reduction of the power supply down to 0.6 V and one of them allows for the reduction all the way down to 0.5 V. With careful design and by using large size devices, the power supply voltage in these three references may be reduced down to 0.5 V.

7.1.3 Simulations

We will provide two best examples of results obtained in simulations.

The first example is the voltage reference using two p-channel transistors with different threshold voltages, and different μC_{ox}. Transistor M_1 is rep-transistor (μC_{ox} = 49 μ A/V^2) with the aspect ratio $(W/L)_1$ = 100/0.5 (here and further in micron/micron), and M_2 is the mep-transistor (μC_{ox} = 104 μ A/V^2) with $(W/L)_2$ = 300/0.5. Resistor R_{S1} = 20 k, the temperature coefficient (TC) of R_{S1} is 1.47E-3. Re-

sistor R_{S2} = 0, the cascoding transistor M_6 is absent. Resistor R_{V1} = 40 k, TC of R_{V1} is also 1.47E-3. Resistor R_{V2} = 40k, TC of R_{V2} is 2.92E-3. Transistors M_3, M_4, and M_5 and M_9, and M_{10} are mep-transistors with the aspect ratio of (300/0.5). The differential amplifier M_7 and M_8 are nan-transistors with the aspect ratio of $(W/L)_{7-8}$ = 100/0.5. The tail current is provided by M_{11} that is also a nan-transistor

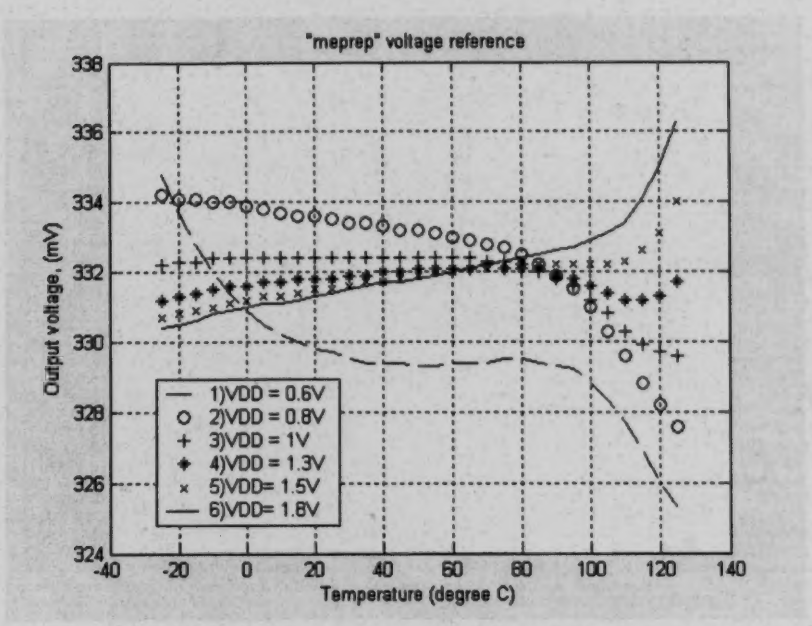

Figure 7.3 Output voltages vs. temperature in the "meprep" voltage reference

with the aspect ratio of $(W/L)_{11}$ = 6/0.5.

The results of simulation for this reference are shown in Figure 7.3. One can see that the variation of the output voltage in the industrial range of temperatures (0 to 75 °C) is less than ± 2 mV (0.6% of V_{out} = 332 mV) for the power supply voltage variation from 1.8 V down to 0.7 V. For a chosen power supply the temperature coefficient of the output voltage is not more than 80 ppm/°C. For the supply voltage of 1 V this figure is about 20 ppm/°C in the full range of temperatures from -25 to 125°C.

The line control of the output voltage is better seen in Figure 7.4 which shows a part of the circuit transient response when the power supply is turned on. It is interesting to see that for this voltage reference, the output voltage initially increases with decreases in the power supply voltage, and only when this voltage diminishes to 0.7 V does the output voltage starts to diminish as well with further decreases in the supply voltage.

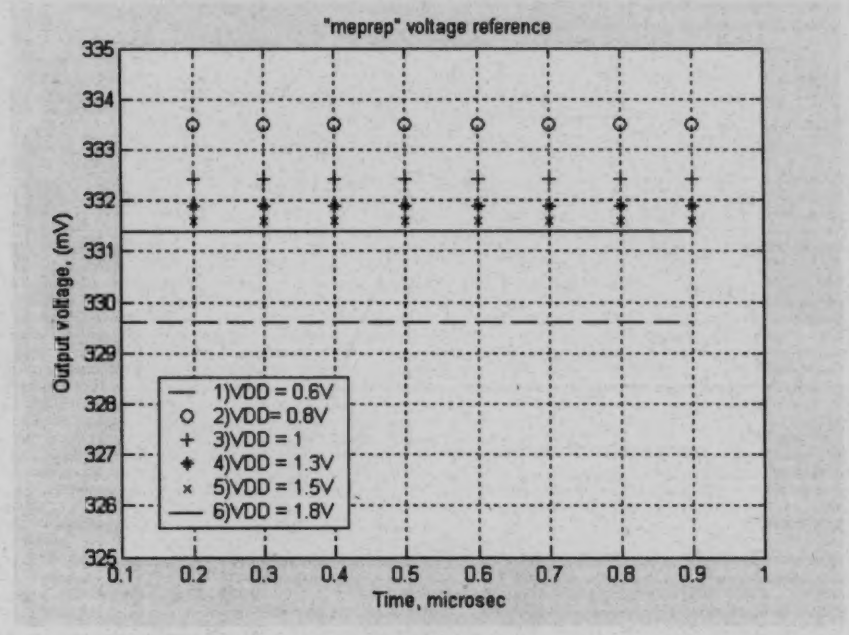

Figure 7.4 Line voltage control in the reference with the same type of transistors

The second example is the voltage reference using one p-channel transistor and one n-channel transistor with different absolute values of threshold voltages. Transistor M_1 is a mep-transistor with an aspect ratio $(W/L)_1$=10/0.5, and M_2 is a nan-transistor with $(W/L)_2$= 50/0.5. Resistor $R_{S1}=R_{S2}$= 8 k, and the temperature coefficient (TC) of R_{S1} and R_{S2} is 1.43E-3. Resistor $R_{V1}=R_{V2}$=32 k, and the temperature coefficient of R_{V1} and R_{V2} is 2.97E-3. Transistors M_3, M_4 and M_5, M_6 and M_9, and M_{10} are mep-transistors with an aspect ratio of (300/0.5). The differential amplifier M_7 and M_8 is formed by nan-transistors with the aspect ratio of $(W/L)_{7-8}$= 50/0.5. The tail

current is provided by M_{11} which is also a nan-transistor with an aspect ratio of $(W/L)_{11} = 10/0.5$.

The results of simulation for this reference are shown in Figure 7.5. As it can be expected the correlation between the threshold voltages of two transistors with the different type of channel is less, and the variation of the output voltage is wider in the same temperature range. In addition, the variation of the output voltage with temperature has different aspect here. The output voltage only decreases from its value at the room temperature. Yet, in the industrial range of temperatures this decrease is about -10 mV (4% of V_{out} =250 mV) for the power supply voltage variation from 1.8 V down to 0.6 V. The circuit is still operable even if the power supply drops down to 0.5 V.

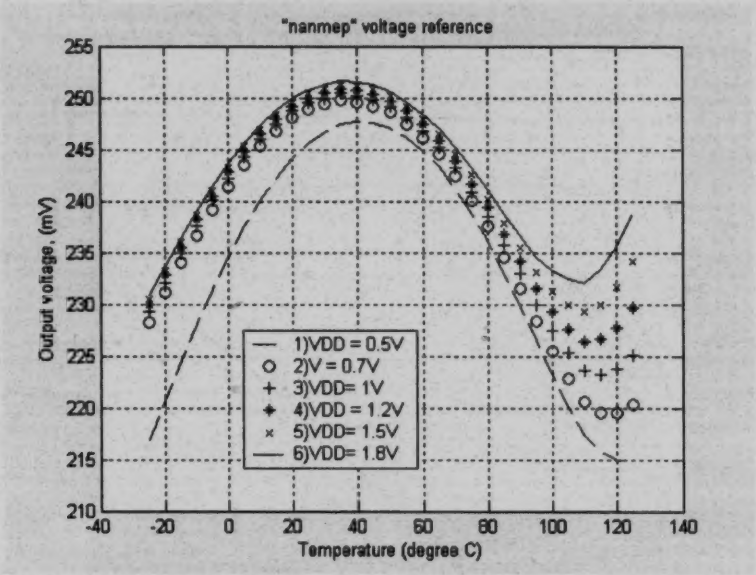

Figure 7.5 Output voltages vs. temperature in "nanmep" voltage reference

The line control of the output voltage for this reference is shown in Figure 7.6. Here the output voltage decreases along with decreases in the supply voltage. This decrease is small (about 2 mV) when the supply voltage drops from 1.8 V down to 0.6 V. A larger decrease of the output voltage is observed when the supply voltage drops below 0.6 V.

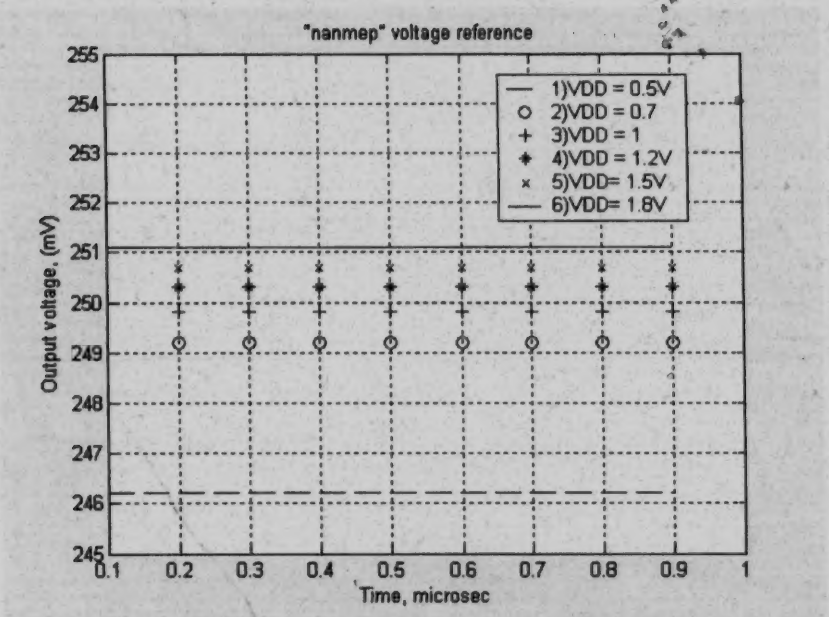

Figure 7.6 Line voltage control in the reference with different type of transistors

7.2 *Blauschild's resistorless voltage reference*

7.2.1 Voltage reference using the direct difference of two threshold voltages

The voltage reference described in this part is using the same architecture as in [60] that allows one to avoid the influence of the operational amplifier offset on the output voltage. This reference can be also realized in the standard 0.18 μ m CMOS technology, on condition that, besides regular n-channel transistors, it also includes the p-channel transistors with reduced threshold values. The proposed reference is using the difference of regular n-channel transistor threshold voltage value, V_{TN} = 0.47 V, and $|V_{TP}|$ = 0.17 V of reduced threshold voltage p-channel transistor.

The design of this voltage reference is based on the same assumptions that were used in the previous part, i.e. that the difference V_{TN} - $|V_{TP}|$ is nearly constant over the wide range of temperatures. We also used the assumption that the mobility of p- and n-channel transistors can track each other, and that the ratio $(\mu C_{ox})_n / (\mu C_{ox})_p$ is nearly constant with temperature as well. The last assumption becomes less important when the current supplied to the reference circuit is reduced, and the reference output voltage becomes closer to V_{TN} - $|V_{TP}|$.

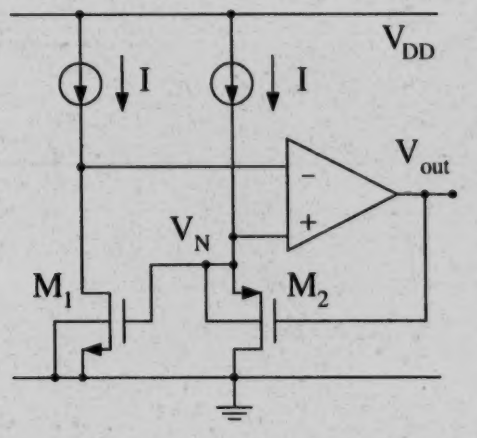

Figure 7.7 The resistor-less voltage reference

The circuit of the proposed reference is shown in Figure 7.7. It includes an operational amplifier that keeps the voltages at the current sources equal. This is achieved by controlling the gate voltage of transistor M_2, and establishing the same currents in M_1 and M_2. Transistors M_1 and M_2 have different absolute values of the threshold voltages. The voltage controlling the gate voltage of M_2 is the reference output voltage.

If the device operation is described by the quadratic law, and the currents in M_1, and M_2 are equal, then

$$V_N = V_{TN} + \sqrt{\frac{2I}{(\mu C_{ox})_n (W/L)_1}} \tag{7-7}$$

and

$$V_N - V_{out} = |V_{TP}| + \sqrt{\frac{2I}{(\mu C_{ox})_p (W/L)_2}} \tag{7-8}$$

One finds that the output voltage is equal to

$$V_{out} = V_{TN} - |V_{TP}| + \sqrt{2I}\left(\frac{1}{\sqrt{(\mu C_{ox})_n (W/L)_1}} - \frac{1}{\sqrt{(\mu C_{ox})_p (W/L)_2}}\right) \tag{7-9}$$

Let the device sizes be chosen so that

$$\frac{(W/L)_2}{(W/L)_1} = \frac{(\mu C_{ox})_n}{(\mu C_{ox})_p} \approx 1.5 \tag{7-10}$$

(numerical value was established simulating individual transistors), then

$$V_{out} = V_{TN} - |V_{TP}| \tag{7-11}$$

and the last difference, as it was established for the devices with larger feature size [45], is nearly constant with temperature.

The quadratic law of the drain current versus gate-source voltage used in derivation (7-7)-(7-11) may be used over a limited range of currents for the devices in submicron technologies. Yet, one can see that with the reduction of current the operation in the quadratic law becomes less important, as well as the matching relationship given by equation (7-10). The output voltage V_{out} is given by (7-11) for any size of transistors.

7.2.2 Voltage reference transistor realization

The transistor realizations chosen for the proposed reference include two circuits.

The first circuit (the core circuit) is shown in Figure 7.8. This circuit was designed to verify that when the external current diminishes, the circuit output voltage is still rather constant, in accordance with (7-11), and does not change with temperature.

This circuit is designed using p-channel transistors with reduced threshold voltage

(transistors M_2 to M_4, and M_7 to M_{10} with $V_{TP} = -0.17$ V, model *mepch*), n-channel transistors with reduced threshold voltage (transistors M_5 and M_6 with $V_{TN} = 0.27$ V, model *mench*), and one n-channel transistor M_1 with the regular threshold of $V_{TN} = 0.47$ V (model *nch*). The transistor aspect ratios are 7/0.5 for M_1 (here and further down in micron/micron), 10/0.5 for M_2, 20/0.5 for M_3 and M_4, 10/0.5 for M_5 and M_6, 6/0.5 for M_7, 9/0.5 for M_8 and M_9, and 12/0.5 for M_{10}.

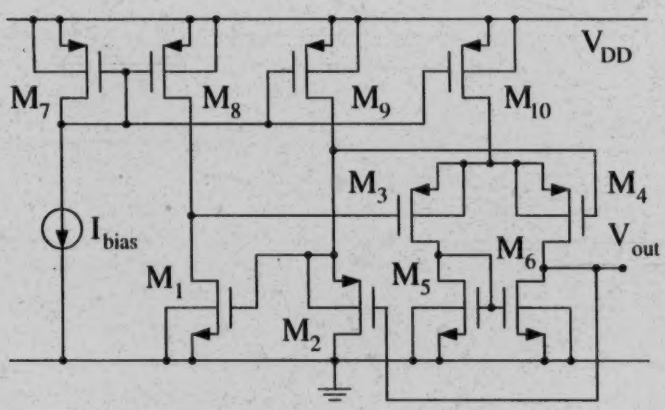

Figure 7.8 Voltage reference core circuit

The second circuit is shown in Figure 7.9. It was designed to evaluate the influence of the frequently used voltage independent bias circuit on the performance of the voltage reference when the power supply voltage is reduced from 1.8 V down to 0.6 V.

In addition to the previous core circuit of Figure 7.8 (with the same type and size of transistors) it includes the standard [26] power supply independent bias circuit (this current source was also considered in Chapter 4) including transistors M_{11} ($V_{TP} = -0.17$ V, model mepch) with the aspect ratio of 6/0.5 and the current mirror M_{12}, M_{13} ($V_{TN} = 0.27$ V, model mench) with the aspect ratio of 10/0.5. Resistor R has the value of 10 k, its temperature coefficient TC=1.47E-3. This bias-circuit

needs a start-up circuit (not shown).

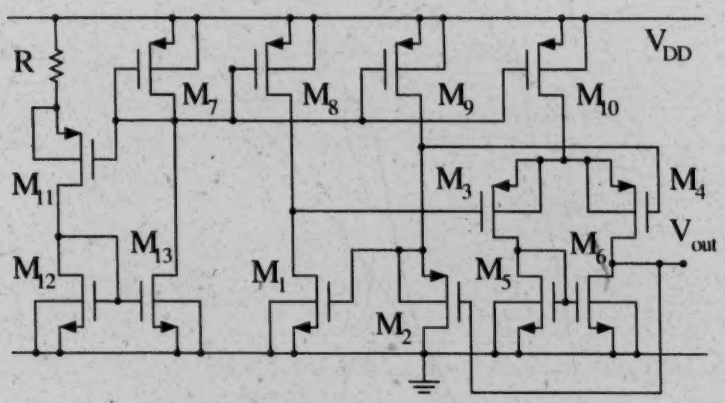

Figure 7.9 Voltage reference with bias circuit

7.2.3 Simulation results

Figure 7.10 shows the results of simulation for the core circuit of Figure 7.8 while the power supply voltage $V_{DD} = 1.8\,\text{V}$ and variation of the supply current from 10 μA down to 0.25 μA. One can see that the core may work with a very low consumption current. Transistors move from strong inversion operation to the weak inversion. Yet the circuit functionality is preserved, and the variation of the output voltage for each value of supply current is not more than 2 mV over the full temperature range of –25 to 125 ^{o}C (i.e. the temperature coefficient is about 58 ppm/^{o}C).

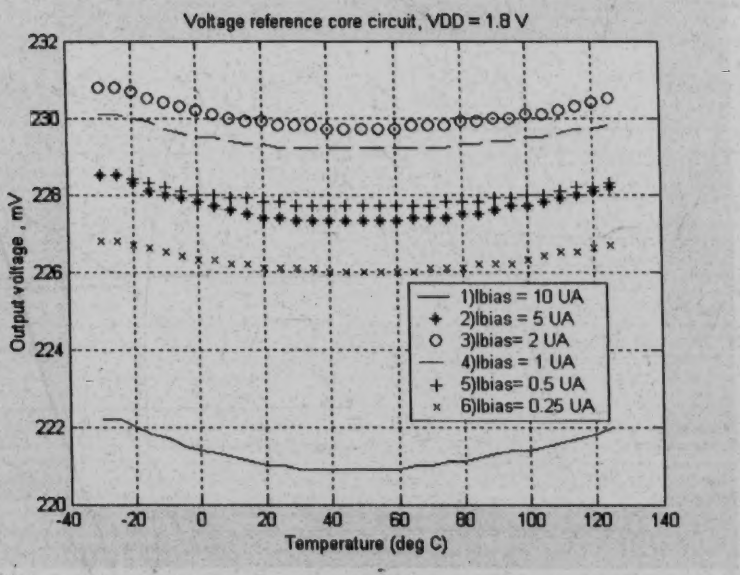

Figure 7.10 Output voltages vs. temperature in core circuit for V_{DD} = 1.8V

The level of output voltage changes with the level of power supply current as well, even though this variation is not big (about 10 mV, or about 4% for 40 times change of the bias current). It is interesting to note that this level initially increases, then achieves a maximum, and then starts to decrease. The explanation of this result requires a more attentive look at the behavior of the circuit in the transition from strong inversion to the region of weak inversion.

The behavior of the output voltage for V_{DD} =0.6 V and variation of supply current is shown in Figure 7.11. One can see that the level of the output voltage is, basically, between the same limits of 230 and 225 mV. For each value of current the output voltage changes again by not more than 2 mV over the same temperature range of –25 to 125 ^{o}C.

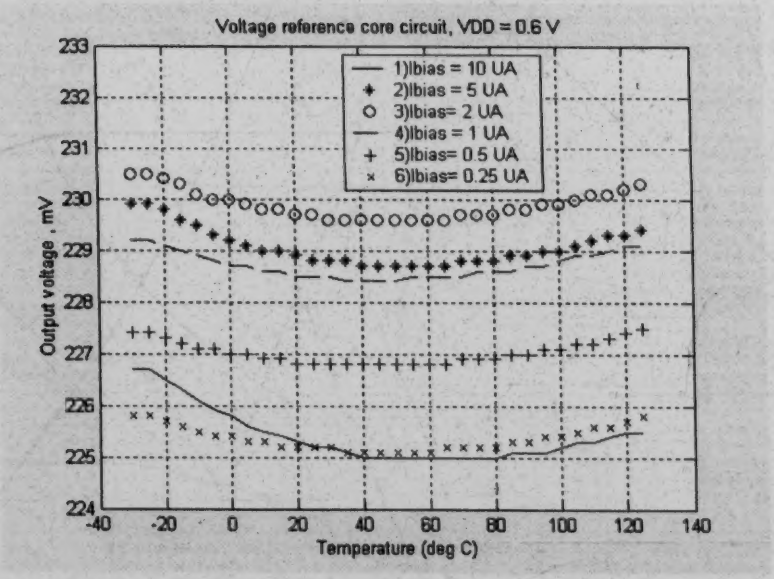

Figure 7.11 Output voltages vs. temperature in core circuit for V_{DD} = 0.6 V

The level of output voltage also changes with the level of power supply voltage. In Figure 7.12 the same pattern, namely, an initial increase and then a subsequent decrease of the output voltage level, is preserved for this power supply voltage as well. Figure 7.12 shows the results of simulation in the voltage reference of Figure 7.9. Here one changes the power supply voltage V_{DD} in the steps of 0.3 V from V_{DD} = 1.8 V down to V_{DD} = 0.6 V. The circuit was simulated over the same range of temperatures –25 to 125 °C. The total variation of the output voltage level is about 8 mV (i.e. it is reduced) and the variation of output for a chosen power supply voltage is also reduced to 1.5 mV over the same temperature range (i.e. the temperature coefficient is reduced to 44 ppm / °C).

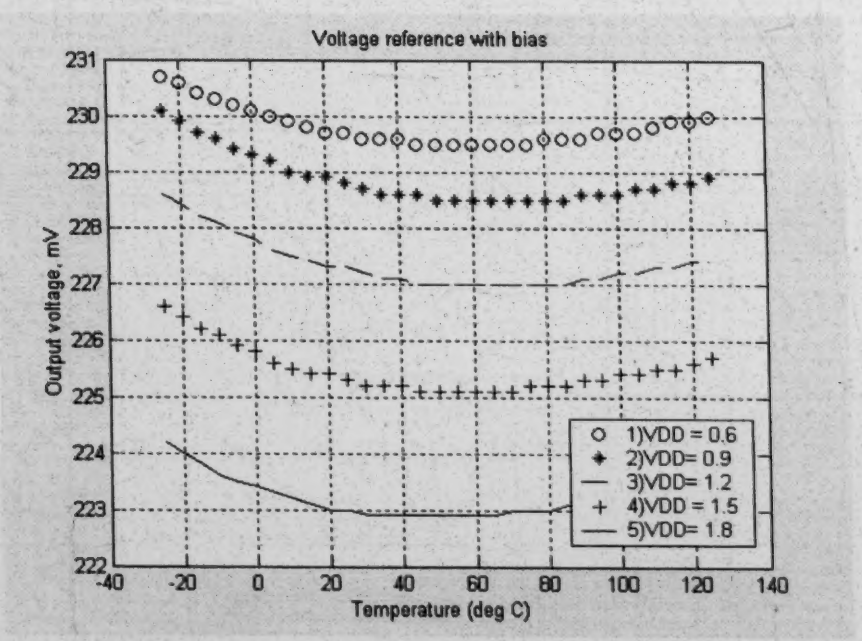

Figure 7.12 Output voltages vs. temperature in the voltage reference with bias circuit

The line regulation of the output voltage for this circuit (about 7 mV) is more clearly seen in Figure 7.13.

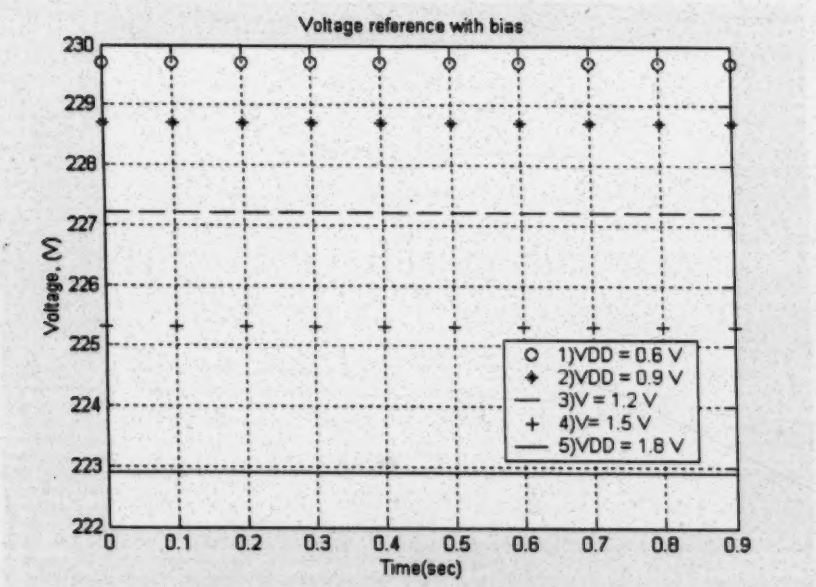

Figure 7.13 Line control of the output voltage in the reference with bias circuit

7.4 Voltage reference using the asymmetric amplifier

7.4.1 Voltage reference structure

The third voltage reference investigated in this chapter is shown in Figure 7.14. This reference is configured as a one-stage asymmetric differential amplifier using rep- and mep-transistors. The active load of this amplifier is a current mirror including two men-transistors. One input of this one-stage amplifier is grounded, and another input is directly connected to the output. It is shown below that in this configuration, one can find the condition when the output voltage will be equal to the difference of the threshold voltage absolute values for p-channel transistors. This difference is temperature-stable as it was proven by the design of the previously considered non-bandgap references. The proposed reference can be easily tuned for optimal operation, and does not require a buffer amplifier.

However, the main reason why this configuration is considered is because it clearly formulates that the problem of references operating with the power supply voltage,

which is equal or below 0.7 V, is equivalent to the problem of finding a circuit that provides a constant current.

7.4.2 Voltage reference operation

In this voltage reference the transistor M_1 has a threshold voltage of V_{THrep} = -0.46 V, M_2 has a threshold voltage of V_{THmep} = -0.17 V. Transistors M_3 and M_4 are both men-transistors with V_{THmen} = 0.27 V. Assume that all transistors are in saturation, and their drain characteristics are described by the quadratic law, as usual.

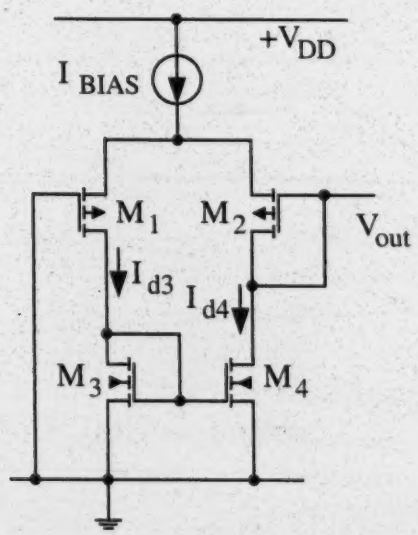

Figure 7.14 Voltage reference circuit using an asymmetric amplifier

Then one has the following relationships:

$$\begin{cases} \dfrac{I_{d3}}{I_{d4}} = \dfrac{(W/L)_3}{(W/L)_4} = a \\ I_{d3} + I_{d4} = I_{BIAS} \end{cases} \quad (7\text{-}12)$$

From these relationships one finds that

$$\begin{cases} I_{d4} = I_{BIAS}/(1+a) \\ I_{d3} = I_{BIAS}\,a/(1+a) \end{cases}, \tag{7-13}$$

The drain currents of transistors M_1 and M_2 are

$$\begin{cases} |I_{d1}| = I_{d3} \\ |I_{d2}| = I_{d4} \end{cases}, \tag{7-14}$$

and one can write that

$$\begin{cases} V_{sg1} = |V_{THrep}| + \sqrt{\dfrac{2I_{d3}}{\mu_{prep} C_{oxrep} (W/L)_1}} \\ V_{sg2} = |V_{THmep}| + \sqrt{\dfrac{2I_{d4}}{\mu_{pmep} C_{oxmep} (W/L)_2}} \end{cases}, \tag{7-15}$$

From (7-15) and (7-12) one can find that

$$V_{out} = V_{REF} = |V_{THrep}| - |V_{THmep}| + \sqrt{\frac{2I_{BIAS}}{1+a}} \left(\sqrt{\frac{a}{\mu_{prep} C_{oxrep} (\frac{W}{L})_1}} - \sqrt{\frac{1}{\mu_{pmep} C_{oxmep} (\frac{W}{L})_2}} \right) \tag{7-16}$$

Hence, if the condition

$$a \frac{\mu_{pmep} C_{oxmep}}{\mu_{prep} C_{oxrep}} = \frac{(W/L)_1}{(W/L)_2} \tag{7-17}$$

is satisfied, one determines that the output voltage

$$V_{out} = V_{REF} = |V_{THrep}| - |V_{THmep}| \tag{7-18}$$

Hence, the output voltage in this reference is equal to the difference of threshold voltage values as in the previous references, and it is temperature-stable.

The proposed configuration is, probably, the simplest one. It relies on the practically geometric relationship between transistor parameters. In addition, it does not include any operational amplifiers because the configuration itself is a one-stage amplifier with 100% feedback. It has a low output impedance and does not need any buffers.

7.4.3 Design procedure

The condition (7-17) includes the geometric relationships between transistor aspect ratios, the ratio of oxide capacitances C_{oxmep}/C_{oxrep}, and the ratio of motilities μ_{pmep}/μ_{prep}. This last relationship deserves some discussion.

Threshold voltage modification is usually achieved by a change of doping concentration in a thin layer of semiconductor directly under the gate. The mobility is a function of temperature, as we know, may be written as

$$\mu = \mu_0 \left(\frac{T_0}{T} \right)^{-m} \tag{7-19}$$

This change of doping concentration changes μ_0, but is not enough to change m. Hence, the relationship (7-17) looks temperature (and bias) independent, and being satisfied at one temperature will be valid at other temperatures as well. This looks too good to be true, and the following factors should be taken into consideration.

1) The derivation assumes that all devices are described by the quadratic dependence of drain current versus overdrive voltage. This is only an approximation, and it is useful before design to simulate a number of individual devices, and to obtain the dependencies $\sqrt{|I_d|} = F(V_{gs} - |V_{TH}|)$. The operating currents should be taken in the middle of the most linear parts of these dependencies. Unfortunately, these points usually do not completely coincide for all transistors, and this introduces the temperature dependence in (7-17).

2) Choose $a = 1$ (why not?), choose the size of the device M_1 so that M_1 and M_2 are in saturation. Changing the ratio $(W/L)_2/(W/L)_1$ one can find the optimal size of M_2. This device is normally much wider than M_1 because the quadratic law region for mep-devices is located at much smaller current densities than for regular devices.

3) Adjust I_{BIAS} to obtain the smallest temperature variation in the output voltage.

4) Design the current source I_{BIAS}. The difference between, say, 0.7 V and $|V_{THrep}| = 0.46$ V provides enough headroom to put inside the effective voltage of M_1

and the required minimal voltage for I_{BIAS}. Sometimes (see the discussion of simulation results) there is a chance to work even with 0.6 V power supply voltage, the tail current sources that require only 50 mV of voltage are known [62].

7.4.4 Simulation results

The simulation results for the circuit of Figure 7.15 are shown in Figure 7.16. Transistors M_3 and M_4 have an aspect ratio of 100µm/0.5µm. Transistor M_1 has an aspect ratio of 20µm/0.5µm, and transistor M_2 has an aspect ratio of 210µm/0.5µm. This last ratio was obtained by simulations, with the goal of minimizing the temperature variation of the output voltage for I_{BIAS} in the range of 5 to 40 µA.

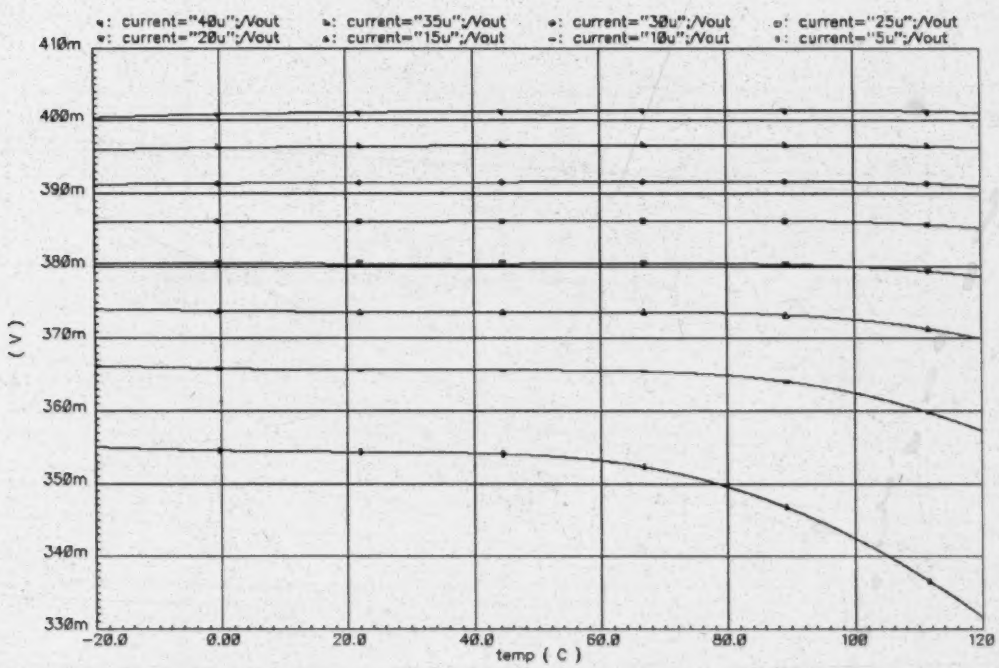

Figure 7.15 Parametric simulation of V_{out} temperature dependence

Figure 7.16 shows separately the dependence $V_{out}(T)$ for I_{BIAS} =30 μA. One can see that in this case the output voltage has a temperature coefficient of 13 ppm/°C over the temperature range -20 to 120 °C.

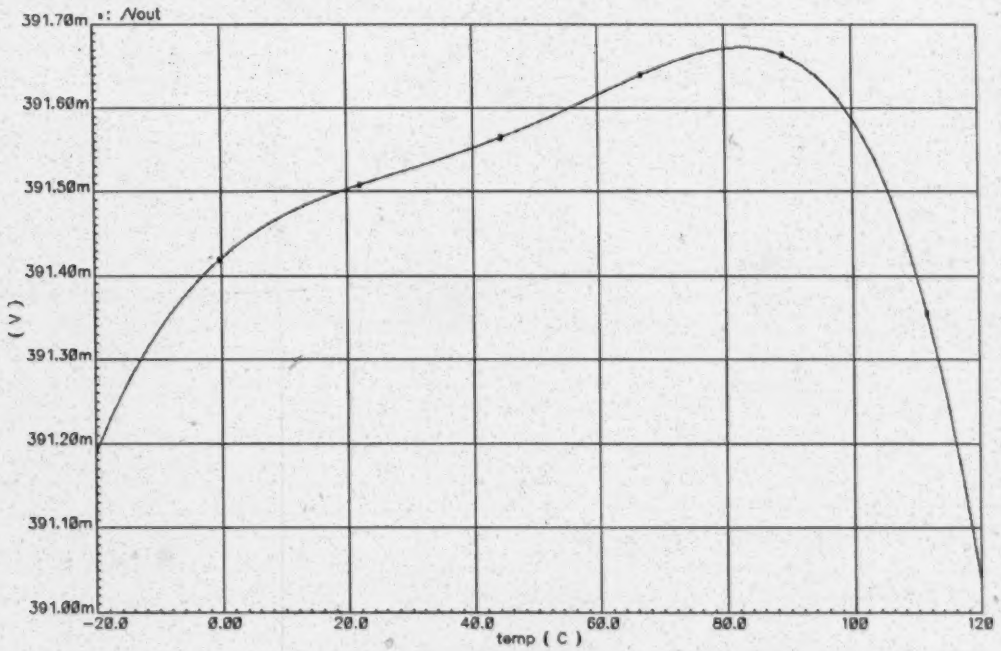

Figure 7.16 V_{out} temperature dependence for I_{BIAS} =30 μA

The results of simulations shown in Figure 7.15 and 7.16 for this non-bandgap voltage reference allow one to formulate quite interesting conclusions. With the power supply equal or below 0.7 V, when the application of bandgap approach is eliminated, the problems of realization of reference voltage and reference current are interchangeable. If one is able to design a temperature-stable current source, then the proposed voltage reference allows one to realize a simple voltage reference. Then an elementary calculation shows that this reference provides voltage variation which is much smaller than, for example, the variation which is obtained by direct application of this constant current to a resistor which is on the chip and which has the best available thermal coefficient.

7.5 Summary

Besides standard transistors, modern 0.18-μm CMOS technology also provides us with transistors that have reduced threshold voltage. This makes it possible to design the voltage reference based on the difference of threshold voltage values.

The mobility in mep- and rep-transistors (or in men- and ren-transistors) track each other sufficiently well to build the references operating at the power supply voltages down to 0.6 V with the output voltage temperature coefficient of about 80 ppm/^{o}C. Over an industrial range of temperatures this figure can be easily reduced to 20 ppm/^{o}C. This means that these nonbandgap references are able to provide the temperature stabilization of the output voltage comparable with that of the first-order, non-curvature-compensated bandgap references.

Using nan- and mep-transistors (or nan- and men-transistors) one can design the references operating at even lower supply voltage of 0.5 V. Yet, the mobility in nan- and mep-transistors (or in nan- and men-transistors) does not track each other so well as in previous cases, and the temperature stability of these references may guarantee their application for bias purposes only.

The Blauschild's resistor-less voltage reference may be designed to consume very small currents. As transistors move from strong to weak inversion operation, this transition does not cause a catastrophic change of the output voltage. A more exact definition of the threshold voltage and its variation with the transistor current is required. This will be a matter of future work.

The simulation results obtained for the asymmetric amplifier type voltage reference show that with power supply voltages below 0.7 V, when any solutions using bandgap approach can not be used any more, the problem of the voltage reference is equivalent to the problem of designing a temperature stable current source.

Chapter 8 Realization of Voltage References Based on Threshold-Voltage-Difference Architecture

As was mentioned before, an essential drop of power-supply voltage for the references was achieved in SOI technology [60]. This technology uses enhancement and depletion mode transistors (i.e. the devices with negative and positive thresholds), and this opportunity does not exist in standard CMOS technologies where all transistors are of the enhancement type. Yet modern CMOS technologies are multi-threshold technologies, and this property may be used for design of voltage references.

The previous chapter shows that for modern 0.18-μ m CMOS technology that has devices with five different thresholds, three types of references are possible. In the first type the voltage equal to the difference of absolute values of two threshold voltages with the help of an operational amplifier is applied to a resistor and converted into a current. This current is supplied, via a current mirror, to an external resistor where the output voltage is formed. In the second type, two equal currents are supplied to two devices with different thresholds, and the operational amplifier (the above mentioned devices may be a part of this amplifier) provides the output voltage equal to the difference of absolute values of two threshold voltages.

Unfortunately, access at the University of Alberta to modern technologies is limited, and in practical design one is limited by the devices with three thresholds, namely, n-channel transistors with V_{TN} = 0.47 V (ren-transistors), p-channel transistors with V_{TP} = -0.46 V (rep-transistors), and n-channel transistors with V_{TN} = 0.03 V (native, or nan-transistors). Two circuits using these types of transistors only were designed, simulated, their layout was done, and the circuits were sent for manufacturing. This chapter describes the results of this design process.

8.1 Voltage reference with resistor

This voltage reference is shown in Fig. 8. 1. The operational amplifier (transistors M5, M7-M10) keeps the voltages applied to the regular n-channel transistor M0 and the branch including the resistors R2, R3 and the native transistor M1 equal. The current developed in this resistor is equal to the drain current of transistor M3. This current is mirrored, first, by the transistor pair M2, M3 to provide the drain current of M0 (hence, M0 and M1 carry equal drain currents), and, second, by the transistor pair M3, M4 to the circuit output. The output voltage is created at resistor R1.

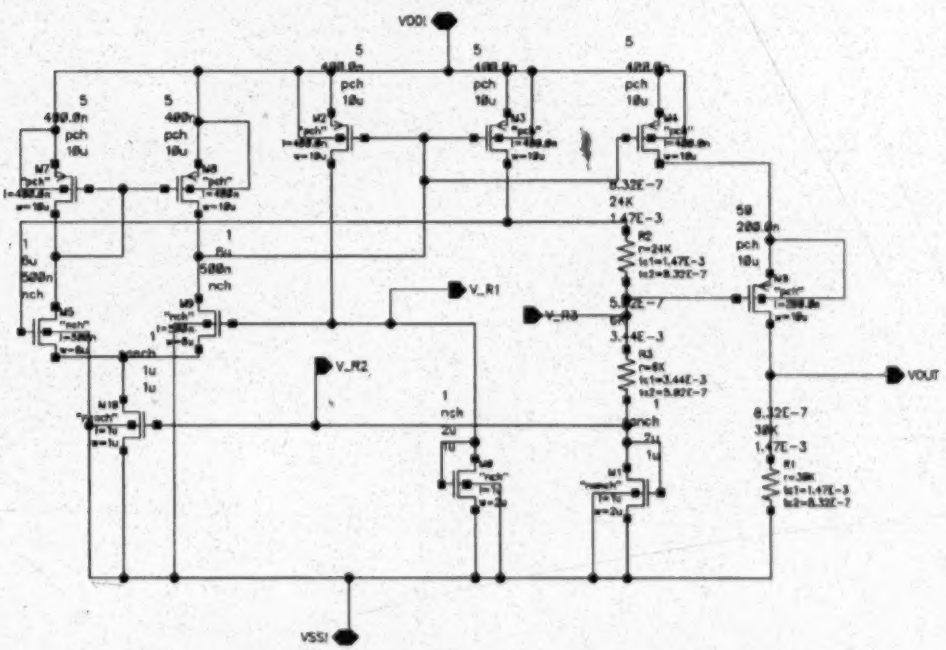

Figure 8.1 The reference with resistors using ren- and nan-transistors

The sizes of transistors M0 and M1 were chosen to satisfy the relationship (7-4), in this particular case that results in equal transistor sizes. Due to the limited lay-out for resistors that CMC provides for us, all the resistors R1, R2 and R3 have to be an N+ diffusion without silicide resistors. The relationship R2+R3=R1 results in the output voltage

$$V_{out} = V_{REF} = V_{Tren} - V_{Tnan} = 0.47\text{-}0.03 = 0.44 \text{ V} \qquad (8\text{-}1)$$

The circuit was simulated, then the layout was done, and the circuit was simulated again, this time from the extracted layout. The result of the simulation from the extracted layout is shown in Figure 8.2. One can see that, indeed, the output voltage satisfies the relationship (8-1), and the output voltage varies around 0.46 V. The lowest power supply voltage where this reference can operate is about 0.9 V. All p-channel transistors in this reference are regular (rep-) transistors, with the threshold of V_{TP} = -0.46 V. The saturation voltage for the chosen transistor sizes is quite high (about 0.35 V), and this value precludes further reduction in the supply voltage.

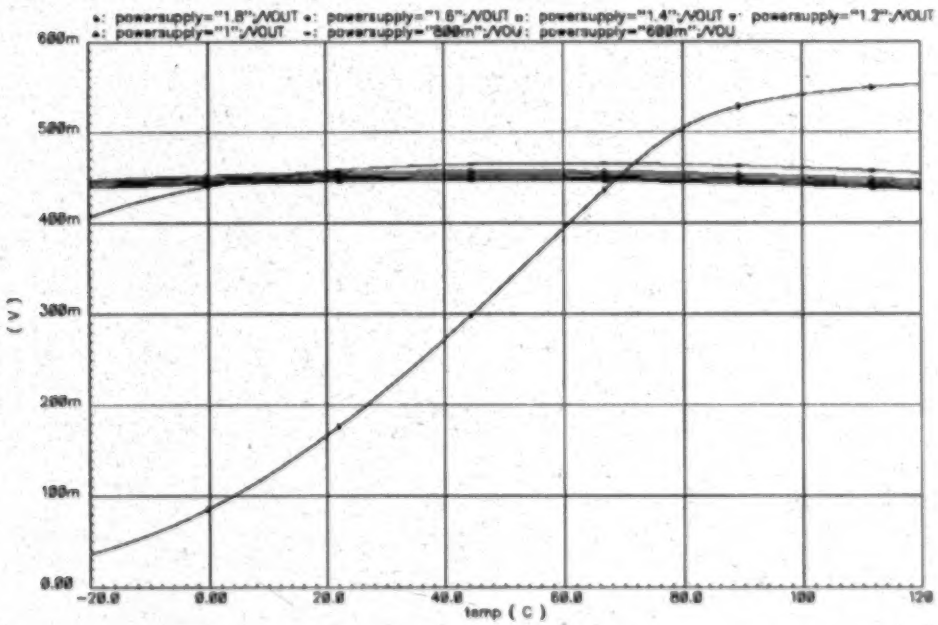

Figure 8.2 Stabilization characteristics of the designed voltage reference

Figure 8.3 shows the reference layout. The circuit occupies an area on 100x100 μ m^2 without pads and the total area with pads is about 310x450 μ m^2.

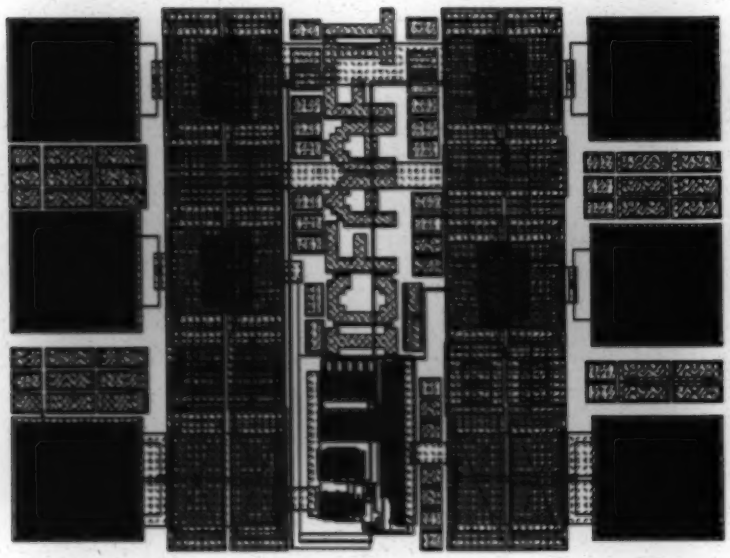

Figure 8.3 The reference layout with resistors

8.2 Resistor-less voltage reference

This voltage reference is shown in Figure 8.4. The current mirrors M16, M13, and M16, M14 provide equal current in the transistors M5 and M0, and the operational amplifier (transistors M6, M9, M10, M12 and M15) controls the source potential of the diode-connected transistor M0. As a result, the gate voltage of M5 is controlled as well. To provide a minimal difference between the input terminals, the operational amplifier was made asymmetric, so that transistor M9 conducts most of the tail current, and the currents in transistors M6 and M12 are equal.

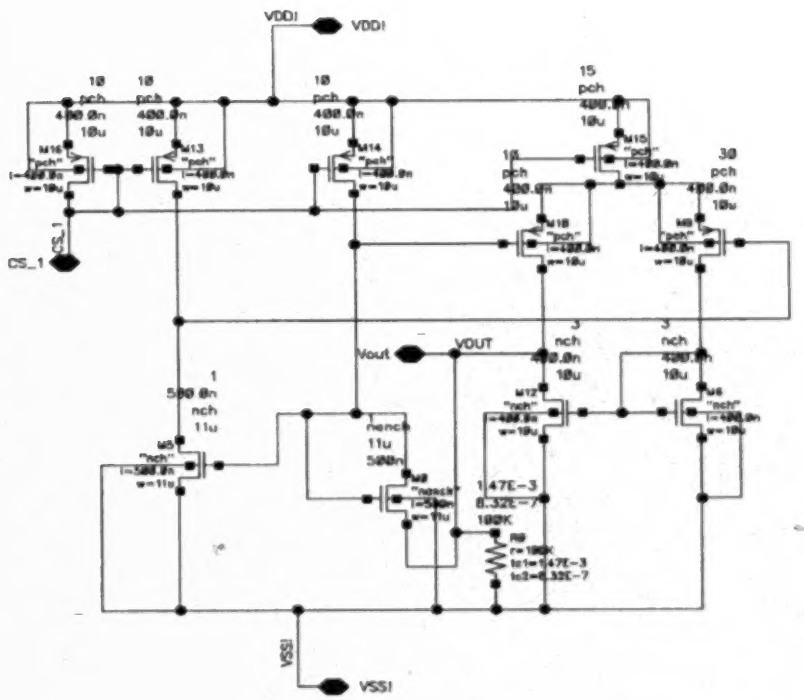

Figure 8.4 Resistor-less voltage reference using ren- and nan- transistors

Under steady-state conditions transistors M5 and M0 carry equal currents. The sizes of transistors M5 and M0 were chosen to satisfy the relationship (7-4), which results again in equal transistor sizes. If one neglects the body effect for the transistor M0, then the output voltage should be

$$V_{out} = V_{REF} = V_{Tren} - V_{Tnan} = 0.47\text{-}0.03 = 0.44 \text{ V} \qquad (8\text{-}2)$$

The circuit was simulated, then the layout was done, and the circuit was simulated again, this time from the extracted layout. The result of the simulation from the extracted layout is shown in Figure 8. 5. One can see that the body effect slightly increases the threshold voltage for the native transistor M0, yet, the output voltage of 0.394 mV is reasonably close to the value given in (8-2).

The lowest power supply voltage where this reference can operate is also about 0.9 V, and for the same reasons. All p-channel transistors in this reference are

regular (rep-) transistors, with the threshold of V_{TP} = -0.46 V. The saturation voltage for the chosen transistor sizes is quite high (about 0.35 V), and this value precludes further reduction of the supply voltage.

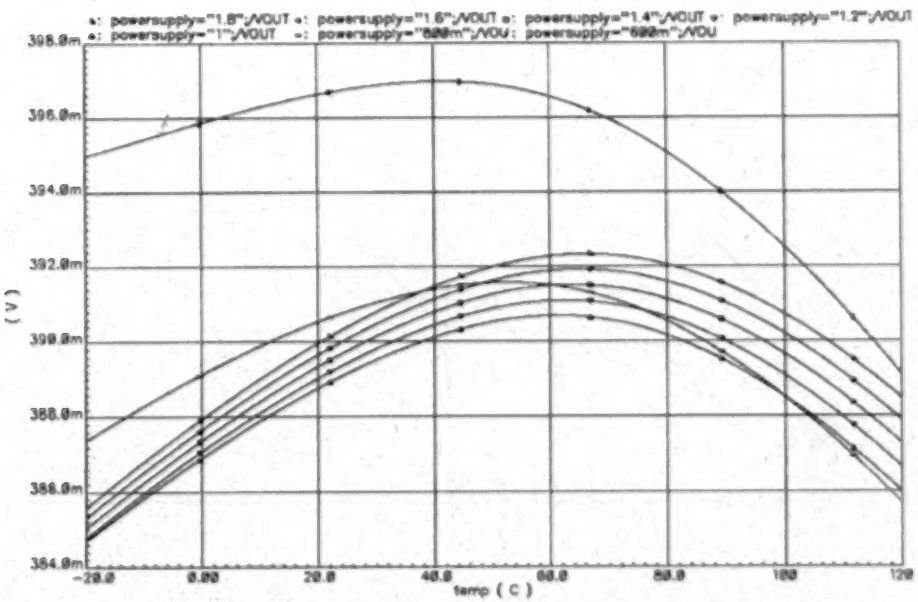

Figure 8.5 The stabilization characteristics of the designed voltage reference.

Figure 8.6 shows the reference layout. The circuit occupies an area on 100x100 μ m^2 without pads and the total area with pads is about 300x300 μ m^2.

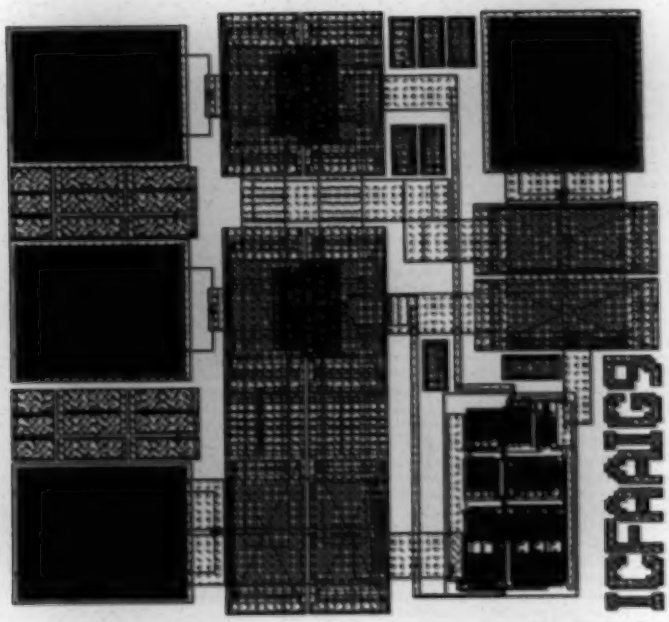

Figure 8.6 The resistor-less voltage reference layout

8.3 Summary

The limited number of different thresholds did not allow us to design the voltage references with the best stability characteristics and lowest power supply voltages further. Yet the results obtained for two designed references allow us to verify the validity of the basic ideas used in their design. The simulations show that the difference of the two threshold voltages for the devices with the same type of channel is relatively stable with temperature. The obtained results show that these references may find application in LDOs, bias circuits, etc.

Chapter 9 Summary and Conclusions

Current and voltage references find applications in a variety of analog and digital circuits and systems. Designing a reference requires the scrutiny of several factors. The temperature dependence of the emitter-base voltage V_{BE} for bipolar transistors, the temperature dependence of the threshold voltage V_{TH} for MOS transistors, and the temperature dependence of mobility $\mu = \mu_0 (T/T_0)^{-\alpha_\mu}$ (especially the exact value of the exponent α_μ) for both bipolar and MOS transistors are important. The first two dependencies are approximately linear and have negative temperature coefficients.

The frequently used first-order bandgap voltage references are designed using temperature compensation of the emitter-base voltage by the amplified thermal voltage $V_T = kT/q$. In direct compensation, the generator of the amplified thermal voltage is connected in series with the emitter-base junction or diode. This results in an output voltage $V_{out} = V_{ref}$ close to the bandgap voltage, which is about 1.25V. The thermal stability of V_{ref} in this case is very high: it is around 10 to 30 ppm/^{o}C. The power supply voltage for such references should be about 1.5 V.

When the compensation is achieved indirectly, say, by generating currents proportional to V_{BE} and V_T, then adding these currents, and applying the result to a resistor, the power supply voltage may be reduced. But the bandgap voltage references are bipolar in nature, even if they are realized in MOS technologies using parasitic bipolar transistors. They require, hence, that the power supply voltage be higher than the V_{BE} voltage, which in practice is about 0.9 V. The output voltage for this type of bandgap reference is less temperature stable. The temperature stability of V_{ref} in this case is about 30 to 100 ppm/^{o}C.

The thermal stability of the output voltage for both types of bandgap references may be improved if one uses currents with more suitable temperature dependence to bias transistors or diodes which provide the V_{BE} voltage, one part of V_{ref}. The most fre-

quently and easily obtained current reference has the current proportional-to-absolute temperature (PTAT current). If a current proportional to the square of absolute temperature ($PTAT^2$ reference) is used for biasing, the thermal stability of V_{ref} improves. Using complicated dependencies of the bias current in high-order bandgap references one may achieve thermal stabilities of V_{ref} in the range of 3 to 10 ppm/^oC. Yet, these improvements do not help to reduce the power supply voltage, and in fact usually require an increase in the supply voltage.

When the power supply voltage is equal to or below 0.7 V, one has to abandon the solutions that were found in the design of bandgap voltage references and to look for some alternatives. Some of them were investigated before, and this thesis investigates further opportunities.

In MOS technologies one can design the voltage references using mutual compensation of mobility and threshold voltage temperature effects. The power supply voltage in these references may be reduced below 1 V. This is not sufficient for some modern applications, yet, the high thermal stability of 4 ppm/^oC obtained in simulations for the output voltage in these references confirms that one may design high quality references of the nonbandgap type.

An essential reduction of power supply voltage may be achieved in multi-threshold MOS technologies. This thesis investigates the nonbandgap references using the difference of two threshold voltages. It shows that, at the present time, the achieved stability of the output voltage is close to that of the bandgap references with reduced power supply voltage. Yet, in the references using the difference of threshold voltages, the power supply voltage may be reduced below 0.6 V.

The main contributions of this thesis are highlighted below.

1. A group of new voltage references where the voltage $||V_{T1}|-|V_{T2}|$ is applied to a resistor was investigated. The current mirror is used to transfer the current in this resistor to the output resistor. The voltage developed at the output resistor is proportional to the difference $|V_{T1}|-|V_{T2}|$ of two threshold voltages. Different reference voltages are obtained by substituting different transistors in the same basic circuit. The tempera-

ture coefficient of the reference voltage in this case may be in the range of 20 to 40ppm/°C.

2. A second type of the reference, similar to the one proposed in [60], was investigated. The reference in [60] is realized in expensive SOI technology, and requires that, similar to [7], transistors with channel depletion are also available. In CMOS technology the reference similar to this type, and investigated in this thesis, can be realized using enhancement transistors only. One of these transistors is of the regular type, with V_{TN} = 0.47V; another is a medium threshold transistor with $|V_{TP}|$ = 0.17V. The current mirror establishes two equal currents in these transistors of different thresholds, and an operational amplifier keeps this condition. The stability of the output voltage in this reference can also be about 20 to 40 ppm/ °C.

3. Finally, the third reference is also an original design. It uses an asymmetric differential pair loaded by an asymmetric active load. This one-stage amplifier has 100% feedback around it. The output voltage of this amplifier is equal to the difference of the gate-source voltages of two transistors with different thresholds. If the tail current of this amplifier is constant, the output voltage of the amplifier has a weak temperature dependence and can be used as a reference voltage. With a stable bias current source the stability can be as good as 13 ppm/ °C.

4. At the time of writing, two reference circuits have been submitted to CMC for fabrication, and the chips will arrive in January for testing and measurements.

The investigation of all these references enables us to formulate some key problems in design of voltage reference operating with power supply voltages below 0.7 V.

When the application of bandgap approach is eliminated, the problems of realizing reference voltage and reference current are interchangeable. If one is able to design a temperature stable current source then the proposed voltage reference allows one to realize a simple voltage reference.

The second key problem for the design of this type of voltage references is finding a circuit that is able to generate the PTAT voltage. In the bandgap references this voltage is usually obtained by using the difference of two V_{BE} voltages. The reduction of the power supply voltage below 0.6 V eliminates this possibility. One may try to use

circuits operating in the subthreshold region. If the corresponding circuits are found one may compensate the temperature dependence of V_{TH} voltage using methods similar to that ones used in the simple first-order bandgap references. One may also develop even more complicated methods as in high-order bandgap references.

The investigation of these two key problems could be pursued as future work.

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